List of Figures

1.1 Switches in Multiprocessors and Multicomputers 2

1.2 Output Port Contention 4

1.3 The ComCoBB Chip 6

3.1 Switch Types 37

4.1 Latency vs. Throughput 61

4.2 Blocking Switches, Varying Buffer Sizes 62

5.1 Variance of Latency, FIFO Switches 69

5.2 Priority Arbitration Performance 73

5.3 Priority Queue, Various Percentages of High-Priority Packets 75

5.4 Increasing Levels of Support for High-Priority Packets 77

5.5 Priority Queue, DAMQ Buffer Efficiency 78

5.6 Impact of Varying Buffer Size, DAMQ Buffers 80

5.7 Five-Queue and Eight-Queue DAMQ Buffers 82

5.8 Varying Percentage of High-Priority Packets 84

5.9 Dedicated Buffers for High-Priority Packets 88

6.1 Synchronous vs. Asynchronous Protocols, Omega Network 100

6.2 Self-Synchronizing DAMQ Switches 105

6.3 Lat. vs. Thpt., Variable-Length Packets 108

6.4 Saturation Throughput vs. Buffer Size, Constant-Length Packets 110

6.5 Saturation Throughput vs. Buffer Size, Variable-Length Packets 111

6.6 Switch for Two-Dimensional Torus 114

6.7 Multi-Queue Buffer for Two-Dimensional Torus 115

6.8 Latency vs. Throughput, 121-Node 2-D Torus 118

6.9 Latency vs. Throughput, 441-Node 2-D Torus 119

6.10 Visualizing Buffer Utilization I 121

6.11 Visualizing Buffer Utilization II 122

6.12 Visualizing Buffer Utilization III 123

7.1 Linked Lists via Buffer Blocks 134

7.2 DAMQ Chip Control Logic 136

7.3 Addressing Phase 137

7.4 Data Movement Phase 138

7.5 The Header Register Array 142

7.6 Memory Cell 147

7.7 Memory Array Read Latency 149

7.8 Buses and Associated Logic for the Head/Tail Register Array 150

7.9 Head / Tail Registers 151

7.10 Block Decoder 152

7.11 Null Register Read Latency 153

7.12 Pointer Register Array 154

7.13 Pointer Register to Tail Register Latency 155

7.14 Latency of Temporary Register to Pointer, Head and Tail Register 156

7.15 Finite State Machine Circuit 158

7.16 Interface to Router and Arbiter 160

7.17 *SYNC* Signal Generator 161

7.18 DAMQ Buffer Floorplan 165

8.1 Network Congestion 169

8.2 Tree Saturation 170

8.3 Operation of Destination-Based Flow Control 184

8.4 Block Diagram, Two-Counter Flow Control 192

8.5 Throughput and Latency, Uniform Traffic Distribution 202

8.6 Benchmark I: Hot Spot, Serial Requests 206

8.7 Benchmark I: FIFO Buffers, Blocking Flow Control 208

8.8 Benchmark I: DAMQ Buffers, Blocking Flow Control 210

8.9 Benchmark I: Maximum-Usage Flow Control 212

8.10 Benchmark I: Two-Counter Flow Control 214

8.11 Benchmark I: Link-Based Flow Control 215

8.12 Benchmark II: Static Hot Spot, Barrier Traffic 217

8.13 Benchmark II: FIFO and DAMQ Buffers, Blocking Flow

Control 219

8.14 Benchmark II: Maximum-Usage Flow Control, Group 0 220

8.15 Benchmark II: Two-Counter Flow Control, Group 0 222

8.16 Benchmark II: Link-Based Flow Control, Group 0 223

8.17 Benchmark III: Non-Uniform Traffic Spot 226

8.18 Benchmark III: FIFO and DAMQ Buffers, Blocking Flow Control 227

8.19 Benchmark III: Maximum Usage Flow Control, Group 0 229

8.20 Benchmark III: Two-Counter Flow Control, Group 0 230

8.21 Benchmark III: Link-Based Flow Control, Group 0 231

8.22 Benchmark IV: Dynamic Serial Transmission 234

8.23 Benchmark IV: DAMQ Buffers, Blocking Flow Control 235

8.24 Benchmark IV: DAMQ Buffers, Maximum-Usage Flow Control 237

8.25 Benchmark IV: DAMQ Buffers, Two-Counter Flow Control 238

8.26 Benchmark IV: DAMQ Buffers, Link-Based Flow Control 239

8.27 Benchmark V: Blocking Flow Control 242

8.28 Benchmark V: Maximum Usage Flow Control 244

8.29 Benchmark V: Two-Counter Flow Control 246

8.30 Benchmark V: Link-Based Flow Control 248

8.31 Benchmark VI: Maximum Usage and Two-Counter Flow Control 250

8.32 Benchmark VI: Link-Based Flow Control 252

8.33 Benchmark I: Group 0 Performance, Combined Flow Control 256

8.34 Benchmark II: Combined Flow Control, Group 0 257

8.35 Benchmark III: Combined Flow Control, Group 0 258

8.36 Benchmark IV: Combined Flow Control, Group 0 259

8.37 Benchmark V: Combined Flow Control 260

8.38 Benchmark VI: Combined Flow Control 261

8.39 Benchmark VI: Destination-Based Flow Control with SAMQ Buffers 263

8.40 Benchmark VI: Destination-Based Flow Control, Suppressed at Destination 265

8.41 Crossbar Hardware for Blocking Flow Control 269

8.42 Crosspoint Controller Hardware for Queue-Based Flow Control 272

8.43 Evaluating Link-Based Flow Control Enhancements: Benchmark VI 277

8.44 Evaluating Link-Based Flow Control Enhancements: Benchmark II 278