Table of Contents

Chapter One - Introduction 1

1.1. Latency and Output Port Contention 3

1.2. The Dynamically Allocated, Multi-Queue Buffer 6

1.3. The Scope of this Work 8

Chapter Two - Previous Work 13

2.1. The Optimal Number of Ports 14

2.2. Buffer Size and Location 15

2.3. Network Contention and Flow Control 21

2.4. Switch Architectures 26

2.4.1. The Post Office Switch 26

2.4.2. The Torus Routing Chip 27

2.4.3. The McMillen Switch Architectures 29

2.5. Buffer Organization via Linked Lists 30

Chapter Three - The DAMQ Buffer Architecture 31

3.1. Switch Size 32

3.2. Buffer Location 33

3.3. Buffer Size and Structure 36

3.4. Buffer Features 41

3.5. Supporting Multiple Classes of Packets 43

Chapter Four - Buffer Performance Evaluation with Synchronous Networks 45

4.1. Synchronous and Asynchronous Networks 47

4.2. Evaluation of 2×2 Discarding Switches Using Markov Models 48

4.3. The Simulator 53

4.4. Evaluation of Discarding Switches via Event-Driven Simulation 56

4.5. Evaluation of Blocking Switches via Event-Driven Simulation 58

4.6. Non-Uniform (Hot Spot) Traffic 63

4.7. Summary and Conclusions 66

Chapter Five - Supporting High-Priority Traffic 67

5.1. Arbiter Support for High-Priority Packets 71

5.2. Dedicated Queues for High-Priority Traffic 72

5.3. Multiple Dedicated Queues for High-Priority Traffic 81

5.4. Dedicated Buffers for High-Priority Traffic 85

5.5. Summary: Support for High-Priority Traffic 89

Chapter Six - Buffer Performance Evaluation with Asynchronous Networks 92

6.1. Simulating an Asynchronous System 93

6.1.1. Network Architecture 93

6.1.2. Packet Injection Parameters 96

6.1.3. Sender Grouping 98

6.2. DAMQ Buffer Performance: Asynchronous MIN 99

6.2.1. Constant-Length Packets, Asynchronous Network 99

6.2.2. Self-Synchronizing Networks 103

6.2.3. Variable-Length Packets, Asynchronous Network 107

6.2.4. Network Throughput with Increased Buffer Memory 109

6.2.5. Summary: Asynchronous MIN Performance 111

6.3. Network Performance, Torus Topology 112

6.3.1. Dimensional Routing with the Multi-Queue Buffers 113

6.3.2. Performance Evaluation: Dimensional Routing 117

6.3.3. Summary — Dimensional Routing 124

6.4. Summary 125

Chapter Seven - The DAMQ Buffer Chip 129

7.1. The Architecture and Microarchitecture of the DAMQ Buffer Chip 131

7.1.1. The Basic Organization of the DAMQ Buffer Chip 133

7.1.2. The DAMQ Buffer Chip Control Logic 135

7.1.3. Minimizing Virtual Cut-Through Latency 139

7.1.4. Summary — DAMQ Buffer Architecture 145

7.2. Floorplan and Circuit Performance 145

7.2.1. The Memory Array 147

7.2.2. The Buffer Control Data Path 150

7.2.3. The Finite State Machines 157

7.2.3.1. The FSM Circuit 157

7.2.3.2. Demand Multiplexing 159

7.2.4. The Floorplan 165

7.3. Summary and Conclusions 166

Chapter Eight - Flow Control 168

8.1. Flow Control Mechanism Taxonomy 173

8.2. Selected Existing Flow Control Mechanisms 174

8.2.1. Hop-Level, Blocking Flow Control 175

8.2.2. End-to-End Flow Control 176

8.2.3. Global Flow Control 180

8.2.4. Discarding, Hop-Level Flow Control 183

8.3. Flow Control Schemes for Tightly-Coupled Interconnection Networks 185

8.4. Hop-Level Flow Control 188

8.4.1. Blocking Flow Control 189

8.4.2. Maximum Usage Flow Control 190

8.4.3. Two-Counter Flow Control 192

8.4.4. Destination-Based Flow Control 195

8.4.5. Path-Based Flow Control 197
8.5. Flow Control Performance Evaluation 198
8.5.1. The Simulator 198
8.5.2. Evaluation Methodology 200
8.5.3. Confidence Intervals 204
8.5.4. Benchmark I: Static Hot Spot, Serial Requests 206
8.5.5. Benchmark II: Static Hot Spot, Many Participants 216
8.5.6. Benchmark III: Static NUT Spot 225
8.5.7. Benchmark IV: Four Senders with Long Messages 233
8.5.8. Benchmark V: 128 Senders Transmitting Multi-Packet Messages 241
8.5.9. Benchmark VI: Uniform Traffic 249
8.5.10. Combining Hop-Level Flow Control Mechanisms 252
8.6. Flow Control Mechanism Implementation 267
8.6.1. Blocking Flow Control 267
8.6.2. Queue-Based Flow Control 270
8.6.3. Destination- and Path-Based Flow Control 273
8.7. Flow Control: Summary and Conclusions 280
Chapter Nine - Summary and Conclusions 284
Bibliography 292