Computer Science Department Technical Report University of California Los Angeles, CA 90024-1596

ON THE INTRINSIC RENT PARAMETER AND SPECTRA-BASED PARTITIONING METHODOLOGIES

L. Hagen

A. B. Kahng

F. J. Kurdahi

C. Ramachandran

March 1992

CSD-920007

On the Intrinsic Rent Parameter and Spectra-Based Partitioning Methodologies*

L. Hagen, A. B. Kahng, F. J. Kurdahit and C. Ramachandrant

UCLA CS Dept., Los Angeles, CA 90024-1596 † UCI ECE Dept., Irvine, CA 92717

Abstract

The complexity of circuit designs has necessitated a top-down approach to layout synthesis. A large body of work shows that a good partitioning hierarchy, as measured by the associated Rent parameter, will correspond to an area-efficient layout. We define the *intrinsic* Rent parameter of a netlist to be a lower bound on the Rent parameter of any partitioning hierarchy for the netlist. Experimental results show that spectra-based ratio cut partitioning methods yield partitioning hierarchies with the lowest observed Rent parameter over all benchmarks and over all algorithms tested. For examples where the intrinsic Rent parameter is known, spectral ratio cut partitioning yields a Rent parameter essentially identical to this theoretical optimum. We provide additional analysis supporting the close relationship between spectral partitioning and the intrinsic Rent parameter. These results have deep implications with respect to both the choice of partitioning algorithms and new approaches to layout area estimation.

1 Introduction

As VLSI system complexity and the number of implementation alternatives continue to increase, top-down approaches have been widely adopted in layout synthesis. Recursive calls to a partitioning algorithm will generate a circuit hierarchy that is typically used either to guide the placement/routing phases of layout, or to afford early estimates of circuit layout area and wireability. The partitioning process is essentially used to discover the natural circuit structure, i.e., a hierarchy of subcircuits such that connectivity between subcircuits is minimized.

Traditional metrics for measuring the quality of a partitioning algorithm analyze the number of nets cut by a 2-way partition of a benchmark circuit. However, these metrics fail to capture the integral role played by the partitioning algorithm in an *overall* layout synthesis or area estimation process – i.e., via its recursive top-down application. Since the quality of the partitioning hierarchy has a direct bearing on the quality of the layout, we would like to find the partitioning strategy that generates the best hierarchy of

^{*}This work was supported in part by NSF MIP-9110696, NSF MIP-8909677, and a SIGDA Graduate Fellowship.

subcircuits. In this work, we propose using the *Rent parameter*, which is a well-established quality measure for the generated layout hierarchy, as a quality measure for the underlying partitioning algorithm itself.

The Rent parameter [28] captures a power-law relationship between the number of external terminals of a subcircuit in the layout and the number of modules in the subcircuit. This parameter has been extensively studied in the field of area estimation, where it affords quite accurate predictions of the wiring requirements for a given partitioning hierarchy. In particular, given two recursive bipartitioning hierarchies for a design, choosing the one with lower Rent parameter will lead to less wirelength and consequently a denser final layout. The Rent parameter is therefore well suited as a quality measure for the complete hierarchy of subcircuits generated by a particular partitioning algorithm.

Our work compares various partitioning algorithms with respect to the Rent parameters of their induced partitioning hierarchies, with the goal of identifying the partitioning strategy whose hierarchy is closest to optimal. To this end, we introduce the notion of an *intrinsic* Rent parameter of a given netlist: the intrinsic Rent parameter is the greatest lower bound or the infimum on the Rent parameter of any partitioning hierarchy for the netlist. Such a lower bound gives a measure of the *required* layout area, independent of layout strategy. An added advantage of this approach is that it affords a new methodology for comparing the utility of partitioning algorithms which is independent of possible differences between the algorithms' individual objective functions.

Our extensive experimental results show that so-called spectra-based partitioning algorithms (i.e., methods based on computing eigenvalues and eigenvectors of a particular netlist-derived matrix) are significantly superior to traditional iterative methods such as the Fiduccia-Mattheyses k-opt approach. Specifically, we have found that an algorithm which recursively partitions an eigenvector-derived linear ordering of the modules to minimize the ratio cut objective yields a partitioning hierarchy which has Rent parameter uniformly better than that of any other method over all benchmark circuits tested. Moreover, with each test case for which the intrinsic Rent parameter is known, the spectra-based ratio cut partitioning hierarchy has Rent parameter essentially identical to the theoretical lower bound.

This result has key implications in two areas. First, it affirms previous work of Wei and Cheng [40], who were the first to propose the ratio cut metric as a partitioning objective, and of Hagen and Kahng [15], who proposed using the spectral approach for ratio cut partitioning. Second, our work naturally leads to the development of better predictive layout models, enabling a more efficient search of the space of layout solutions.

Experimental data in Section 4 below show that spectral ratio cut partitioning is demonstrably preferable to other algorithms in building the layout hierarchy. Given this conclusion, our second avenue of inquiry in this paper pursues a theoretical relationship between the spectral properties and the intrinsic Rent parameter of a given netlist. We describe Rent's relationship as a natural outgrowth of ratio cut partitioning and the ratio cut cost function. Based on this relationship, we show that Rent's parameter can be analytically related to the theoretically derived lower bound on the ratio cut metric presented in [15]. Extensive experiments confirm this relationship, giving further evidence of the close relationship between spectra-based partitioning and the optimal Rent parameter.

The remainder of this paper is organized as follows. Section 2 reviews the use of Rent's rule for wireability analysis and area estimation, and defines both the algorithm-dependent Rent parameter and the intrinsic Rent parameter for a design. Section 3 provides a taxonomy of partitioning algorithms, concentrating on those which are most useful for both hierarchical layout and rapid area estimation applications. Section 4 presents experimental results concerning the intrinsic Rent parameter and shows the relative merits of various partitioning algorithms with respect to their induced Rent parameters. New theoretical results in Section 5 connect the intrinsic Rent parameter with spectral properties of the netlist, thus providing retrospective support for the conclusions of Section 4. The paper concludes in Section 6 with directions for future research.

2 Rent's Rule

Rent's rule is an empirical relation observed in "good" layouts; it reflects a power-law scaling of the number of external terminals of a given subcircuit with the number of modules in the subcircuit. Specifically,

$$T = k \cdot C^p \tag{1}$$

where T is the average number of external terminals (pins) in a subcircuit or partition; k is Rent's constant, a scaling constant which empirically corresponds to the average number of terminals per module; C is the number of modules in the subcircuit (or partition); and p is the Rent parameter or Rent exponent, with $0 \le p \le 1$.

This relation was first observed by E. F. Rent of IBM in the late 1960s and independently by several others, e.g., Donath [4] derived the same relation from a stochastic model of a hierarchical design process. Landman and Russo [28] performed an extensive study of the relation via partitioning experiments on large "real-life" circuits, and observed Rent parameter values p between 0.47 and 0.75. Following Mandelbrot [30]

¹Landman and Russo also observed that Rent's rule is actually a two-region relationship: the power law relation (1) above

and Keyes [20], one may view Rent's rule as a dimensionality relationship between pinout of a module and the number of gates in the module. This is in some sense a surface area to volume relationship where, for example, "intrinsically 2-dimensional" circuits such as memory arrays, PLAs, or meshes will have optimal layouts with p=1/2. Kurdahi and Parker [26] have noted that a Rent parameter value p>0.5 implies that wires must grow longer as circuit size increases; in other words, such a circuit cannot be embedded in two dimensions without "dilation", and the relative contribution of wiring to layout area will grow with the size of the circuit. For example, a 3-dimensional mesh topology requires a layout having $p \ge 2/3$ [25], and indeed such a topology cannot be embedded in the plane without the introduction of long wires. Note that the tractability of the intrinsic Rent parameter analysis for meshes will allow us to use 2-D and 3-D meshes as supplementary benchmarks for which the intrinsic Rent parameter is known.

The value of the Rent parameter strongly affects the layout area of a given circuit. Donath and Feuer [5] and [10] proposed and experimentally verified relationships between the Rent parameter and the average wire length. Their work shows that a lower Rent parameter will result in lower average wire length, which in turn generally implies smaller wiring area and less congestion in the layout.² These results motivate our use of the Rent parameter for a given partitioning hierarchy as a measure of the quality for the corresponding partitioning algorithm.

Landman and Russo in [28] also made the fundamental observation that the Rent parameter will depend upon both the structure of the circuit and the partitioning algorithm chosen. This observation leads to the notion of an algorithm-dependent Rent parameter, which we may denote as $p_H(C)$ to indicate that the Rent parameter p is a function of both the circuit design C and the partitioning heuristic H. In other words, realizations of a given design will have differing Rent parameters depending on the underlying partitioning approach; correspondingly, any hierarchical partitioning algorithm will yield a family of Rent parameter values over the space of logic designs. With this in mind, the present work proposes the notion of an intrinsic Rent parameter, denoted by p^* , which is the minimum Rent parameter attained over all hierarchical decompositions of a given circuit. The intrinsic Rent parameter $p^*(C)$ is thus the infimum of the set of all possible $p_H(C)$ values.

holds in region I, while region II is governed by a more complex relation. In our work, as in [28], we consider scaling laws fitted to the region I domain (cf. the discussion in Section 4.1 below). We also note that in a subsequent paper [32], Russo concluded that, for a given fixed partitioning algorithm, p tends to be high for high performance circuits, and low for low performance circuits. As simple examples, consider that p = 0 for a shift register in which data is loaded serially, and p = 1 for a latch circuit where data is loaded in parallel.

²Cf. the practical wirelength estimation approaches of Donath, Feuer, and Sastry [5] [10] [34], which involve Rent-based analysis. Wirelength estimates are intimately tied to layout wireability analysis [9] [17], and moreover form the basis of analytic area estimation methods, e.g., El Gamal, Heller, Kurdahi, and Sastry [8] [18] [26] [33], which are typically used to complement constructive approaches [27].

A motivating hypothesis for our work has been that the algorithm-dependent Rent parameter can be used to characterize the quality of a given partitioning heuristic H with respect to the given input. As will be seen below, different partitioning algorithms indeed yield widely varying Rent parameters for any given circuit, implying that the wirelength depends considerably on the choice of the partitioning algorithm used in the layout process. Moreover, our experimental results demonstrate that the relative ordering of algorithm-dependent Rent parameters is very consistent across a variety of benchmark circuits. The Rent parameter can thus be used to objectively select among partitioning heuristics for use in a hierarchical layout approach. Before presenting experimental results, we briefly review a taxonomy of those partitioning algorithms which are of interest in the dual contexts of hierarchical layout and rapid area estimation.

3 A Partitioning Taxonomy

A general model for VLSI layout associates a hypergraph H = (V, E') with the circuit netlist; vertices in V represent modules and edges in E' represent signal nets. Several standard transformations [29] may be used to convert H into a graph G = (V, E) with vertices and edges of G weighted to reflect module areas and the multiplicity or importance of connections. Two widely used partitioning formulations are:

- Minimum-Cut Bisection: Given G = (V, E), find the partition of V into disjoint U and W, with |U| = |W|, such that e(U, W), i.e., the number of edges in $\{(u, w) \in E \mid u \in U \text{ and } w \in W\}$, is minimized.
- Minimum Ratio Cut: Given G = (V, E), find the partition of V into disjoint U and W such that $\frac{e(U, W)}{|U| \cdot |W|}$ is minimized.

Because minimum-cut bisection divides module area evenly, it is a popular objective within the hierarchical layout paradigm. However, the area bisection requirement is unnecessarily restrictive and can preclude finding natural structure within the circuit. Various ad hoc thresholds and penalty functions (e.g., the r-bipartition formulation of Fiduccia and Mattheyses [11]) have not been completely successful in relaxing this constraint. With this in mind, the ratio cut formulation [39] provides a more straightforward tradeoff between nets cut and evenness in the partition: the numerator captures the minimum-cut criterion while the denominator favors near-bisection. It is well known that both minimum-cut bisection and minimum ratio cut are NP-complete [13], so heuristic methods must be used. Previous approaches fall into several classes,

as surveyed in [6] [15] [29].³

The greedy iterative paradigm is popular either as a stand-alone strategy or as a postprocessing refinement to other methods. Iterative methods are based on local perturbation of the current solution and typically entail variations of the Kernighan-Lin method [19] [35], e.g., the algorithmic speedups of Fiduccia and Mattheyses [11] and Krishnamurthy [24]. Practical implementations will use a number of random starting configurations and return the best result [29] [39] in order to adequately search the solution space and give predictable performance, or "stability". For example, Wei and Cheng [39] propose a ratio cut heuristic that adapts the shifting and group swapping methods of [11] and returns the best of 20 runs. It should be noted that current wireability analysis algorithms rely almost exclusively on Fiduccia-Mattheyses partitioning. This is due to such reasons as: (i) the long history of Kernighan-Lin k-opt methods in physical layout, (ii) the bisection requirement, which is naturally suited to hierarchical decomposition, and (iii) the simplicity of the algorithm implementation. However, while iterative Fiduccia-Mattheyses style optimization is very fast for single runs and has been a very popular approach, certain limitations loom as problem sizes grow large. These include theoretical results on the weakness of local-search methods, as well as instability and the lack of error bounds; all of these factors seem endemic to the local strategy.

With respect to the present work, an important class of partitioning algorithms consists of efficient "spectral" methods which use eigenvalues or eigenvectors of matrices derived from the netlist graph. Recall that the circuit netlist may be represented by the simple undirected graph G = (V, E) with |V| = n vertices v_1, \ldots, v_n . Often, we use the $n \times n$ adjacency matrix A = A(G), where $A_{ij} = 1$ if $\{v_i, v_j\} \in E$ and $A_{ij} = 0$ otherwise. If G has weighted edges, then A_{ij} is equal to the weight of $\{v_i, v_j\} \in E$, and by convention $A_{ii} = 0$ for all $i = 1, \ldots, n$. If we let $d(v_i)$ denote the degree of node v_i (i.e., the sum of the weights of all edges incident to v_i), we obtain the $n \times n$ diagonal degree matrix D defined by $D_{ii} = d(v_i)$. The eigenvalues and eigenvectors of such matrices are the subject of the relatively recent subfield of graph theory dealing with graph spectra.

Early theoretical work connecting graph spectra and partitioning is due to Barnes, Donath and Hoffman [1] [6] [7]. More recent eigenvector and eigenvalue methods have dealt with both module placement (Frankle and Karp [12] and Tsay and Kuh [38]) and graph min-cut bisection (Boppana [3] and Blanks [2]). In general, these previous works formulate the partitioning problem as the assignment or placement of nodes into bounded-size clusters or chip locations. The problem is then transformed into a quadratic optimization, and

³The reader will note that our discussion omits several popular approaches, including simulated annealing [21] [36], genetic algorithms [23], and relaxation-based two-dimensional placement/partitioning (e.g., Gordian [22]). These methods are generally too CPU-intensive to be used as the basis of area estimation and thus lie beyond the scope of our discussion.

Lagrangian relaxation is used to derive an eigenvector formulation.⁴ In [15], Hagen and Kahng established a close relationship between the optimal ratio cut cost and the second smallest eigenvalue of the matrix Q = D - A, where D and A are as defined above:

Theorem 1 (Hagen-Kahng): Given a netlist graph G=(V,E) with adjacency matrix A, diagonal degree matrix D, and |V|=n, the second smallest eigenvalue λ of Q=D-A yields a lower bound on the cost c of the optimal ratio cut partition, with $c \geq \frac{\lambda}{n}$.

This result suggests that the eigenvector x corresponding to λ , i.e., the solution of the matrix equation $Qx = \lambda x$, be used to guide the partitioning. For ratio cut partitioning, [15] used x to induce a linear ordering of the modules, and the best "split" in terms of ratio cut cost was returned. To be more specific, the n modules x_i of the eigenvector are sorted to yield an ordering $v = v_1, \ldots, v_n$ of the modules which we call the spectral ordering. The splitting index r, $1 \le r \le n-1$, is then found which yields the best ratio cut cost when modules with index > r were placed in U and modules with index $\le r$ were placed in W. This straightforward construction achieved very significant improvements over previous iterative methods, and also exhibited several desirable traits, including speed, provability, and stability. The spectral method is appealing for its use of global rather than local information, and it moreover provides an inherently spatial embedding of the circuit graph. Because the spectral approach significantly outperforms iterative Fiduccia-Mattheyses style methods [15], Section 4 uses the spectral ordering as the basis for ratio cut partitioning variants.⁵

$$z = \frac{1}{2} \sum_{i=1}^{n} \sum_{j=1}^{n} (x_i - x_j)^2 A_{ij}$$

subject to the constraint $|x| = (x^T x)^{1/2} = 1$, with A_{ij} again equal to the strength of the connection between modules i and j. It can be shown that $z = x^T Q x$, so that to minimize z we may form the Lagrangian

$$L = x^T Q x - \lambda (x^T x - 1).$$

Taking the first partial derivative of L with respect to x and setting it equal to zero yields

$$2Qx - 2\lambda x = 0,$$

and this can rewritten as

$$(Q - \lambda I)x = 0$$

where I is the identity matrix. This is readily recognizable as an eigenvalue formulation for λ , and the eigenvectors of Q are the only nontrivial solutions for x. The minimum eigenvalue 0 gives the uninteresting solution $x = (1/\sqrt{n}, 1/\sqrt{n}, \dots, 1/\sqrt{n})$, and hence the eigenvector corresponding to the second smallest eigenvalue λ is used.

⁵While eigenvalue computations are not cheap, the run-times reported in [15] were actually less than those for the multiple F-M computations needed by, e.g., the RCut1.0 program of Wei and Cheng [40]. Significant algorithmic speedups stem from the need to calculate only a single (the second smallest) eigenvalue of a symmetric matrix. Moreover, netlist graphs tend to be very sparse due to hierarchical circuit organization and degree bounds imposed by the technology fanout limits; this allows

⁴ A prototypical example is the work of Hall [16], which we now outline. This work is particularly relevant since it uses eigenvectors of the same graph-derived matrix Q = D - A (the same D and A defined above) that we utilize. Donath and Hoffman, Boppana, and others use different matrices derived from the netlist graph, but exploit similar mathematical properties (e.g., symmetry, positive-definiteness) to derive alternate eigenvalue formulations and relationships to partitioning. Hall's result [16] was that the eigenvectors of the matrix Q = D - A solve the quadratic placement problem of finding the vector $x = (x_1, x_2, \ldots, x_n)$ which minimizes

4 The Intrinsic Rent Parameter

Within the preceding taxonomy, the main classes of partitioning algorithms of interest for top-down layout generation and area estimation are greedy iterative methods (in particular, Fiduccia-Mattheyses minimum-cut bisection) and methods that are based on the spectral ordering. Within these classes, we parameterize the algorithms of interest by (i) their objective function: min-cut metric or ratio cut metric; and (ii) the balance restrictions in the output bipartition: exact bisection, 1/4 - 3/4 range limited, or no limits on range. The following is a list of the algorithms used in our experiments:

- 1. SpecRC-Full: spectral ordering; partition the ordering at best splitting point by ratio cut metric.
- 2. SpecRC-1/4: spectral ordering; partition the ordering at best splitting point by ratio cut metric, subject to constraint that maximum partition size is $\leq \frac{3}{4} \cdot |V|$.
- 3. Spec-Bis: spectral ordering; bisect the ordering. In other words, this is simply "spectral bisection".
- 4. FM-1/4: Fiduccia-Mattheyses implementation of the Kernighan-Lin method for minimum net cut partitioning; range limitation ("r" in [11]) such that maximum partition size is $\leq \frac{3}{4} \cdot |V|$.
- 5. FM-Bis: "standard" Fiduccia-Mattheyses method, i.e., for minimum net cut bisection.⁶

To generate a control for these partitioning strategies (and, separately, to confirm the work of Sutherland and Ostreicher [32] [37], who posit a Rent parameter of 1 for random partitioning methods), we also tested the following three variants of random circuit partitioning:

- 6. RandMC-1/4: random linear ordering; partition this linear ordering at best splitting point by minimum net cut metric, subject to constraint that maximum partition size is $\leq \frac{3}{4} \cdot |V|$.
- 7. RandRC-1/4: random linear ordering; partition this linear ordering at best splitting point by ratio cut metric, subject to constraint that maximum partition size is $\leq \frac{3}{4} \cdot |V|$.
- 8. Rand-Bis: random linear ordering; bisect this linear ordering.

application of sparse numerical techniques such as the block Lanczos algorithm [14].

⁶Since the computation time required for spectral-based partitioning is slightly more than that for FM-based partitioning [15], we (over-) compensated the CPU expense by selecting the FM-based Rent parameter as the minimum over 10 independently generated FM-based partitioning hierarchies.

All eight partitioning strategies were tested on the three circuits Primary1, Primary2 and Struct from the MCNC benchmark suite. We also used two highly structured inputs as additional benchmarks: Mesh2D, a 2-dimensional mesh topology, and Mesh3D, a three-dimensional mesh topology. Since Primary1 and Primary2 are circuits with unknown structure, little can be deduced about their intrinsic Rent parameter. On the other hand, Struct is an array multiplier with a mesh-like topology, meaning that its intrinsic Rent parameter is likely to be 1/2. Additionally, since Mesh2D and Mesh3D have very regular topologies, their respective intrinsic Rent parameters are known to be exactly 1/2 and 2/3; we therefore use these latter benchmarks to assess the near-optimality of various partitioning hierarchies. Table 1 summarizes the characteristics of the benchmark circuits.

Benchmark	cells	nets	pins	pads	cell library	technology
Primary1	752	904	2941	81	sclib	SCell 2-metal
Primary2	2907	3029	11226	107	sclib	SCell 2-metal
Struct	1888	1920	5471	64	db	MOSIS SCMOS
Mesh2d	2000	4090	8000	180	test	test
Mesh3d	1000	3300	6000	600	test	test

Table 1: Benchmark Circuit Characteristics

4.1 Experimental Procedure

Our experimental procedure was as follows. For a given benchmark circuit, each algorithm is used to construct a partitioning hierarchy for the circuit by recursively partitioning the circuit and its subpartitions until all subpartitions contained less than 9 modules. At each partitioning step, we note the size and number of external pins for each subpartition. A high-level template for this phase is given in Figure 1.

Generate-Partitions(P)
Input: A circuit netlist P
if $ P \geq 9$
partition P into subpartitions P_U and P_W
output size and number of pins for P_U and P_W
$\operatorname{Generate-Partition}(P_U)$
Generate-Partition (P_W)

Figure 1: Algorithm to generate partitioning hierarchy.

We next establish *levels* within the partitioning hierarchy such that each level contains a set of disjoint subpartitions of roughly equal size. Intuitively, each level can be viewed as a "bucket" that contains some

subset of the subpartitions generated during the recursive partitioning process. By computing the average size and the average number of pins for the subpartitions in each partition level, we obtain the data points which yield the Rent parameter via regression analysis.

Given the complete partitioning hierarchy, we have two distinct methods for generating the partition levels. With method (i), we traverse the partitioning hierarchy in a breadth-first manner; thus, a partition level consists of all subpartitions at a given depth (distance from the root) in the hierarchy. With method (ii), we define a partition level to be a set of k subpartitions containing all modules, subject to the constraint that the maximum size of any subpartition is minimum. Thus, method (ii) derives partition levels by traversing the partitioning hierarchy according to the algorithm described in Figure 2: given partition level P_k with k subpartitions, the algorithm constructs partition level P_{k+1} with k+1 subpartitions by replacing the largest subpartition in P_k with its two children in the hierarchy.

Partition-Level-Generator()							
Input: A partitioning hierarchy							
let P = complete circuit							
let A = P							
while P is partitioned in the hierarchy							
A = A - P							
$A = A \cup \text{ partitions of } P$							
Output A							
P = largest element of A							

Figure 2: Traversal (ii) algorithm for determining partition levels.

For a partitioning hierarchy based on bisection, the partition levels produced by traversal (i) will be a subset of the partition levels of traversal (ii). However, as the balance restrictions are loosened, the two traversals give different results. Using traversal (i), the lower levels may include only a subset of the circuit if previous levels contain subpartitions that are leaves. On the other hand, any traversal (ii) level will always include the complete circuit, and moreover for 1/4 - 3/4 range limited partitioning the ratio between the largest and smallest subpartitions in any given level will be less than or equal to three.

In order to correlate the experimental data to Rent's rule, we re-express the relationship $T = k\dot{C}^p$ as $\log T = \log k + p \cdot \log C$, which is a straight line equation with intercept $\log k$ and slope equal to the Rent parameter p. From this formula, we see that the Rent parameter p can be calculated by performing linear regression on the data points plotted on a $\log \log p$ scale. Our plotted data points represent the average⁷

⁷There are two commonly used techniques for calculating averages: geometric and arithmetic. Although previous work has calculated the Rent parameter [28] using arithmetic averaging, we derive the experimental data below using geometric averaging

number of external terminals and modules per subpartition for each partition level.

Last, we followed the methodology described in [28] and divided our data points into two regions: Region I where Rent's rule applies, and Region II (corresponding to the first one or two levels of the hierarchy) where the rule breaks down. The transition from Region II to Region I is found by including in Region I all points which result in a fit where maximum error between actual data and the estimated Rent parameter does not exceed 10%. For traversal (i), in no case were more than the first two levels assigned to Region II. For traversal (ii), we include the number of levels assigned to Region II in the summary of experimental results (Table 3 below).

The Region II data can be viewed as the intermediate partitioning steps needed to "explode" the original circuit into a state at which the intrinsic behavior of the partitioning algorithm will manifest itself. Let each partition level i correspond to a data point (C_i, T_i) , where C_i is the average number of modules per subpartition and T_i is the average number of external terminals per subpartition. All partitioning algorithms create hierarchies starting at the same point (C_0, T_0) (the complete circuit) and ending at the same point (C_n, T_n) (where C_n is equal to 1 and T_n is the average number of external terminals per module). Therefore, in order for their Rent parameters to vary, there must be a stage (Region II) early in the partitioning hierarchy where the ratio $\log(C_i)/\log(T_i)$ has non-linear behavior dependent on the partitioning algorithm. This initial behavior causes the starting point of Region I to vary with each partitioning algorithm, and consequently each partitioning algorithm will approach (C_n, T_n) with distinct slope (i.e., Rent parameter) on the log-log plot.

4.2 Experimental Results

Fitted Rent parameters for all of the variant partitioning hierarchies are summarized in Tables 2 and 3. The experimental data shows that an algorithm-dependent Rent parameter is indeed derivable for all of our tested variants, including the random partitioning methods. Since the results for all the Rand variants gave essentially identical Rent parameters we chose Rand-Bis as a representative from this category to compare with the other partitioning algorithms.⁸

at each partition level. This is due to the following reasons. First, taking an arithmetic average of the observed data on the log-log scale corresponds to taking a geometric average of the original data points, i.e. geometric averaging of the experimental data gives a more "natural" average on the log-log scale. Second, as will be shown below in Section 5, a theoretical relationship between spectral based ratio cut partitioning and the Rent parameter hinges on the use of geometric averaging techniques. Finally, all previous work that we are aware of concerning the derivation of Rent's relationship has been based on bisection methods. Clearly, the distinction between geometric and arithmetic averaging is irrelevant vis-a-vis bisections, and the analysis given in previous work holds with either averaging method. Thus, our choice of geometric averaging in no way precludes direct incorporation of our results within the existing body of work on Rent's parameter.

⁸Note that the Rent parameters for all bisection variants should be the same using either traversal (i) or (ii); however, slight differences result from the fact that the traversal (i) data points used in the regression are a subset of the data points used to

Partitioning	Rent parameter (p)									
strategy	Primary1	Primary2	Struct	Mesh2d	Mesh3d					
Rand-Bis	.880	.931	.923	.942	.936					
FM-Bis	.736	.794	.848	.681	.689					
FM-1/4	.606	.736	.713	.573	.691					
Spec-Bis	.660	.706	.598	.524	.613					
SpecRC-1/4	.396	.640	.516	.554	.655					
SpecRC-Full	.196	.491	.510	.546	.666					

Table 2: Rent parameter results using traversal (i).

Partitioning	Rent parameter (p)									
strategy	Primary1	Primary2	Struct	Mesh2d	Mesh3d					
Rand-Bis	.916 (2)	.951 (2)	.935 (2)	.970 (2)	.953 (2)					
FM-Bis	.723 (2)	.933 (1)	.878 (2)	.663 (2)	.711 (1)					
FM-1/4	.670(2)	.772 (2)	726 (3)	.563(1)	.720(1)					
Spec-Bis	.662 (1)	.693 (6)	.635(5)	.514 (0)	.620 (0)					
SpecRC-1/4	.574 (5)	.658 (7)	.580 (4)	.540 (2)	.654 (0)					
SpecRC-Full	.456 (7)	.617 (6)	.572 (3)	.524(1)	.660 (0)					

Table 3: Rent parameter results using traversal (ii). Numbers in parentheses show the points belonging to Region II.

Occasional entries in these tables are derived from regressions of fewer data points, and may have lesser statistical significance. However, the results clearly indicate that our experimental methodology effectively distinguishes the relative merits of the various partitioning methods. In particular, the spectral ratio cut variants SpecRC-1/4 and SpecRC-Full generate partitioning hierarchies with uniformly superior Rent parameters for all test circuits. For Struct and the mesh inputs, where we know the value of the intrinsic Rent parameter, we see that SpecRC-1/4 and SpecRC-Full give partitioning hierarchies with Rent parameters very close to the optimal values of 1/2 for Struct and Mesh2d, and 2/3 for Mesh3d. Notice also that our experiments support the conjecture of Sutherland and Ostreicher [37] in that they yield Rent parameters very close to 1 for random partitioning hierarchies on all circuits.

Last, we note that our conclusions are strengthened when we take into consideration the quality of the fit between our data and the regressed line. Figures 3, 4, 5 and 6 show graphs depicting the data points and their regressed lines for the Struct and Primary2 benchmarks, using each of the traversals (i) and (ii). Since traversal (ii) generates so many levels, the graphs show only one out of every 10 data points; however, the regression analysis was done on all the points. The goodness of fit was measured using a correlation calculate the Rent parameter for traversal (ii). An example of this phenomenon is shown for the Spec-Bis variant.

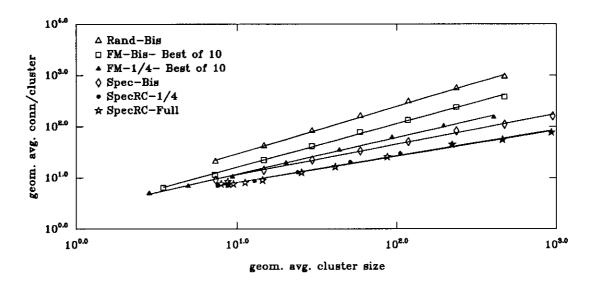


Figure 3: Rent's rule fit for Struct using traversal (i)

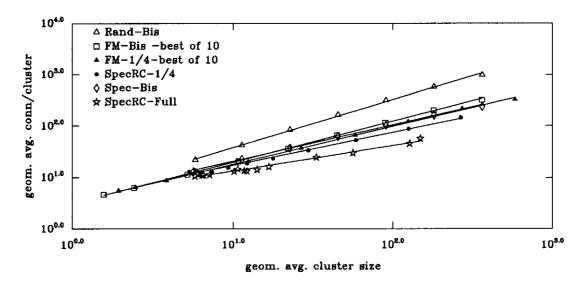


Figure 4: Rent's rule fit for Primary2 using traversal (i)

coefficient [31]. Virtually every example had correlation coefficient higher than .98, indicating a consistently good fit.⁹

⁹The sole exception: Primary1 with traversal (i) for SpecRC-Full, where the fit was done on only five data points.

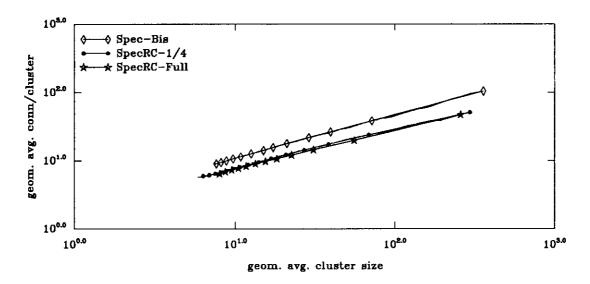


Figure 5: Rent's rule fit for Struct using traversal (ii)

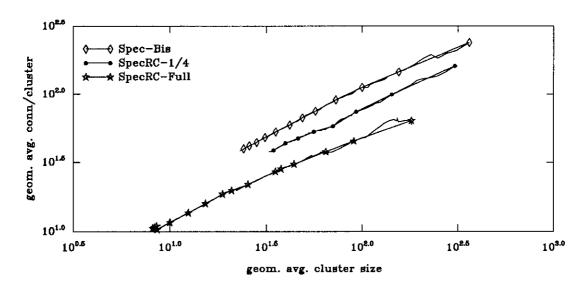


Figure 6: Rent's rule fit for Primary2 using traversal (ii)

4.3 Speedups for Estimating the Rent Parameter

The methodology described above uses the entire partitioning hierarchy to compute the Rent parameter p. Deriving this hierarchy can be very time consuming and might thus defeat the purpose of using Rent's relationship in the first place, particularly if our application happens to involve early wireability analysis or area estimation. The excellent fit of our data points to the power-law in Rent's relationship suggests the

following method for estimating the Rent parameter: restrict the recursive partitioning to only the first k levels of the hierarchy, then apply the linear regression analysis to that subset of the partitioning data.

In order to achieve a good estimate, we must ensure that the data used in the regression analysis actually belongs to Region I of the partitioning hierarchy. In some cases, this may amount to discarding the first few partition levels from the regression analysis. Table 4 shows the results of applying this k-level approach to traversal (i) data in estimating p for the spectra-based partitioning strategies. For each design and for each partitioning strategy, we show the smallest subranges of data points (i.e. partition levels) that were needed to estimate p within maximum error tolerances of 5% and 10%. The smaller number in each subrange corresponds to the start of Region I. We conclude that with all test cases, significant reduction in computation time, with little corresponding loss of solution quality, will be possible when we restrict the depth of the partitioning. In many cases, p can be estimated within a maximum allowed error of 10% by recursively partitioning to only 4 or 5 levels. We believe that Monte Carlo methods which examine random root-leaf paths in the partitioning hierarchy may similarly be applied to reduce the number of partitions computed.

Rent parameter estimation was also performed using the traversal (ii) data for our benchmarks. We observed that adding data points to the Rent parameter estimate resulted in an essentially monotonic convergence toward the known Rent parameter of the entire partitioning hierarchy. For example, with the Mesh2D benchmark we found that the Spec-Bis, SpecRC-1/4, and SpecRC-Full methods respectively required 40, 49, and 29 partition levels in order to achieve 5% accuracy in the estimate of the Rent parameter. To achieve 10% accuracy, the methods respectively required only 9, 35 and 16 partition levels. Note that the number of partitioning steps required to generate partition level k in traversal (i) is $O(2^k)$, while only O(k') partitioning steps are required to generate partition level k' with traversal (ii). Thus, traversal (ii) also affords very accurate estimates of the Rent parameter after generating only a small fraction of the partitioning hierarchy, and moreover the amounts of work are very comparable between the two traversal methods.

Partitioning	Primary1		Primary2		Struct		Mesh2d		Mesh3d	
strategy	5%	10%	5%	10%	5%	10%	5%	10%	5%	10%
Spec-Bis	2-5	2-5	3-7	3-6	1-5	1-4	1-6	1-4	1-4	1-4
SpecRC-1/4	2-8	2-5	3-6	3-6	1-6	1-5	2-6	2-5	1-4	1-4
SpecRC-Full	3-8	3-8	3-6	3-6	1-5	1-4	1-6	1-4	1-4	1-4

Table 4: Estimating Rent's parameters - Summary of results

5 A λ -Rent Relationship

The empirical results presented above suggest that the smallest Rent parameter is derived when we use the ratio cut metric for partitioning. In view of the proposed concept of an intrinsic Rent parameter, this suggests that the spectral ratio cut approach is in some sense an intrinsically good top-down partitioning strategy. This section presents theoretical arguments and empirical results which support this conclusion.

Given a circuit C, let U and W be the partitions resulting from applying a spectral-based ratio cut partitioning to C. Theorem 1 [15] gives the following lower bound on the value of the ratio cut cost:

$$\frac{e(U,W)}{|U|\cdot|W|} \ge \frac{\lambda}{n} \tag{2}$$

Assuming the optimal ratio cut partition of C achieves the lower bound in (2), we obtain the following relationship:

$$\frac{e(U,W)}{|U|\cdot|W|} = \frac{\lambda}{n} \tag{3}$$

If Rent's rule holds for partitions U and W, then we must also have

$$e(U, W) = k + Avg(|U|, |W|)$$

where Avg(|U|, |W|) denotes the average of |U| and |W|.

Assuming that Avg(|U|, |W|) is computed as the geometric average, we may rewrite Rent's relationship for U and W as

$$e(U, W) = k \left[(|U| \cdot |W|)^{\frac{1}{2}} \right]^{p^*}$$

$$= k \left(|U| \cdot |W| \right)^{\frac{p^*}{2}}$$
(4)

where k is Rent's constant and p^* is the intrinsic Rent parameter. We can also compute e(U, W) from (3) as:

$$e(U, W) = \frac{\lambda}{n}(|U| \cdot |W|) \tag{5}$$

Setting $|U| = x^*$ and equating e(U, W) in (5) and (6), we obtain the approximate relationship

$$\frac{\lambda}{n}x^*(n-x^*) = k[x^*(n-x^*)]^{\frac{p^*}{2}}$$

 \mathbf{or}

$$\frac{\lambda}{n} = k \left[x^* (n - x^*) \right]^{\frac{p^*}{2} - 1} \tag{6}$$

which strongly suggests a close relationship between λ and the intrinsic Rent parameter p^* . Indeed, the relationship (6) may be viewed as a new characterization of the scaling properties of circuit netlists.

To validate the relationship in (6), we performed the following experiment. First, we observe that (6) implies that $\frac{\lambda}{n} = F(x^*(n-x^*))$ can be plotted on a log-log scale as a straight line with a decreasing slope of $\frac{p^*}{2} - 1$. Based on this observation, our task of experimentally validating the relation in (6) is reduced to testing the fit of the partitioning data obtained from our experiments to a straight line on a log-log plot. Because Rent's rule is an average relationship, we average the partitioning data and use one representative average data point for each level of the hierarchy in the fitting test. Given a spectra-based partitioning method (e.g., Spec-Bis, SpecRC-1/4, and SpecRC-Full), we computed $x^*(n-x^*)$ and $\frac{\lambda}{n}$ for each partition level in the partitioning hierarchy. In order to obtain an average point for each level of the hierarchy, we geometrically averaged the x-values (i.e., the $x^*(n-x^*)$ values). Both geometric and arithmetic averaging of the y-values (i.e., $\frac{\lambda}{n}$) were used, with the latter giving much better fits.

For every benchmark circuit, we plotted the data corresponding to Spec-Bis, SpecRC-1/4, and SpecRC-Full. In each case, we performed a linear regression and estimated the slope of the regression line. Only the data which was found to belong to Region I in Rent's relationship (as described in Section 4) was included in the fit. From this data, we used a procedure similar to the one used in Section 4 to locate the region, which we call Region A, where the relationship in Equation (6) is valid; remaining data points comprised Region B. In all the cases, Region B had no more than the first two points of each set (i.e. corresponding to the first two levels). Figures 7, 8, 9, and 10 show typical results using both traversals (i) and (ii). Although the fits are not quite as good as those pertaining to the Rent parameter in Section 4 above, the data gives a clear indication that the relationship in Equation (6) holds.¹⁰

¹⁰There are several sources of error that would potentially affect the goodness of the fit: (1) the relationship derived in Theorem 1 assumes a graph model whereas the circuits are actually hypergraphs with an average net fanout of around 3.5; (2) the relationship in Equation (6) assumes that the lower bound on the ratio cut function predicted by Theorem 1 can be achieved, which may not always be the case; (3) the points on the graph corresponding to the first levels were otained by averaging a very small number of points and thus may not be as statistically significant as other data points; and finally, (4) a

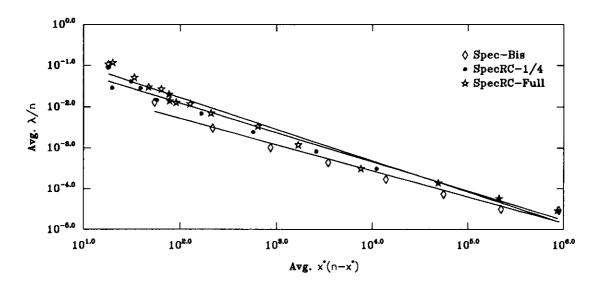


Figure 7: Experimental validation of the λ -Rent relationship for Struct using traversal (i)

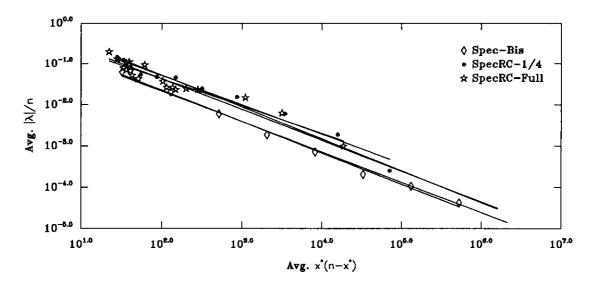


Figure 8: Experimental validation of the λ -Rent relationship for Primary2 using traversal (i)

Tables 5 and 6 compare the slope of the regression line fit to the data and the one predicted by Equation 6 using the estimated Rent parameter from Tables 2 and 3, respectively. We notice that the range of slopes is well within what is predicted by the λ -Rent relationship: if $0 \le p \le 1$, then $-1 \le (\frac{p}{2} - 1) \le -0.5$. All the slopes were in the range [-.99, -.64]. Generally speaking, there is a reasonable agreement between

small percentage (about 10%) of the partitioning data was discarded because the eigenvalue computations resulted in floating point errors.

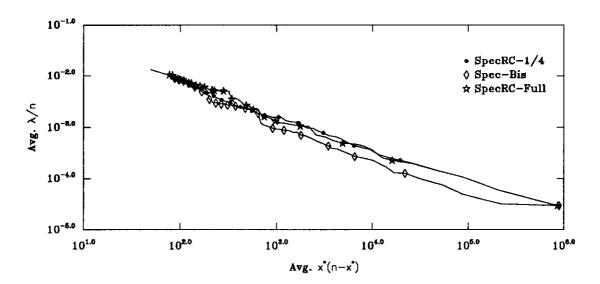


Figure 9: Experimental validation of the λ -Rent relationship for Struct using traversal (ii)

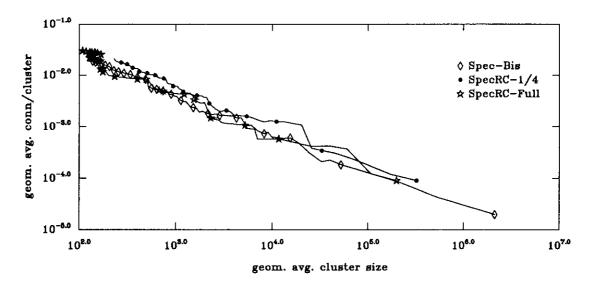


Figure 10: Experimental validation of the λ -Rent relationship for Primary2 using traversal (ii)

the estimated slopes and the predictions based on Rent's relationship. The only exceptions arise with the Mesh2d benchmark, where for SpecRC-Bis and SpecRC-1/4 we find a relatively large difference (about 25%). Overall, the experimental data strongly confirms the relationship proposed in Equation (6).

Partitioning	Primary1		Primary2		Struct		Mesh2d		Mesh3d	
strategy	$\frac{p}{2} - 1$	slope								
Spec-Bis	67	81	65	76	74	64	74	99	69	71
SpecRC-1/4	80	89	68	71	74	72	72	91	67	74
SpecRC-Full	90	90	75	66	75	77	73	73	67	75

Table 5: Experimental validation of the Rent-Eigenvalue relationship using traversal (i) - Summary of results

Partitioning	Primary1		Primary2		Struct		Mesh2d		Mesh3d	
strategy	$\frac{p}{2} - 1$	slope								
Spec-Bis	67	84	65	79	68	77	74	99	69	66
SpecRC-1/4	71	88	67	77	71	65	73	98	68	73
SpecRC-Full	90	90	69	80	71	70	74	76	67	73

Table 6: Experimental validation of the Rent-Eigenvalue relationship using traversal (ii) - Summary of results

6 Conclusions

We have introduced the notion of a circuit's "intrinsic Rent parameter" defined as the lowest Rent parameter achievable by any partitioning method. Our empirical results indicate that spectral based ratio-cut partitioning methods generate partitioning hierarchies whose Rent parameters are lower than those of any other algorithms tested, and which are moreover optimal for those examples where the intrinsic Rent parameter is known. In particular, comparisons of the partitioning hierarchies generated by spectral based and Fiduccia-Mattheyses based partitioning methods show that with all benchmarks the spectral based partitioning hierarchy is superior to the hierarchy generated by Fiduccia-Mattheyses based partitioning. This result suggests that top-down layout techniques based on spectral ratio cut partitioning methods will achieve denser layouts than the current tools based on Fiduccia-Mattheyses style partitioning. Current work addresses the integration of spectra-based ratio cut partitioning into a top-down layout synthesis package.

Our results also imply that tools for layout area estimation and wireability analysis should be based on spectral ratio cut partitioning; such methods will achieve closer estimates of the resources required for a given design. We showed that the Rent parameter of a spectra-based partitioning hierarchy can be closely estimated using only a small subset of the complete hierarchy, e.g., only three or four partition levels using traversal (i). In the context of predictive tools for top-down synthesis, this affords very significant speedups which will enable better exploration of the layout design space.

Finally, we show that there is a close theoretical relationship between λ , the second smallest eigenvalue

of the netlist-derived matrix Q = D - A, and p^* , the intrinsic Rent parameter of the circuit. This approximate relationship is given by the formula $\lambda/n = k \left[x^*(n-x^*)\right]^{\frac{p^*}{2}-1}$. Our empirical analysis of the λ values for partitioning hierarchies generated using spectra-based ratio cut partitioning strongly confirm this relationship. This provides additional support for the notion that the spectra-based partitioning approach will yield a hierarchy with Rent parameter equal to the intrinsic Rent parameter. We are currently pursuing estimation of the intrinsic Rent parameter directly from the λ values of the first few partitioning operations.

References

- [1] E. R. Barnes. An algorithm for partitioning the nodes of a graph. SIAM J. Alg. Disc. Meth., 3(4):541-550, 1982.
- [2] J. Blanks. Partitioning by probability condensation. In Proc. Design Automation Conf., pages 758-761, 1989.
- [3] R. B. Boppana. Eigenvalues and graph bisection: An average case analysis. In *IEEE Symp. on Foundations of Computer Science*, pages 280-285, 1987.
- [4] W. Donath. Hierarchical structure of computers. Technical Report RC 2392, IBM T. J. Watson Res. Cen. Yorktown Heights, N.Y., 1969.
- [5] W. E. Donath. Placement and average interconnection lengths of computer logic. IEEE Transactions on Circuits and Systems, CAS-26(4):272-277, 1979.
- [6] W. E. Donath. Logic partitioning. In B. Preas and M. Lorenzetti, editors, Physical Design Automation of VLSI Systems, pages 65-86. Benjamin Cummings, 1988.
- [7] W. E. Donath and A. J. Hoffman. Lower bounds for the partitioning of graphs. IBM J. Res. Dev., pages 420-425, 1973.
- [8] A. A. El Gamal. Two-dimensional stochastic model for interconnections in master slice integrated circuits. IEEE Transactions on Circuits and Systems, CAS-28(2):127-138, February 1981.
- [9] D. K. Ferry. Interconnection lengths and VLSI. IEEE Circuits and Devices, pages 39-42, July 1985.
- [10] M. Feuer. Connectivity of random logic. IEEE Transactions on Computers, C-31(1):29-33, January 1982.
- [11] C. M. Fiduccia and R. M. Mattheyses. A linear-time heuristic for improving network partitions. In Proc. Design Automation Conf., pages 175-181, 1982.
- [12] J. Frankle and R. M. Karp. Circuit placement and cost bounds by eigenvector decomposition. In Proc. ICCAD-82, pages 414-417, 1982.
- [13] M. R. Garey and D. S. Johnson. Computers and Intractability: A Guide to the Theory of NP-Completeness. Freeman, 1979.
- [14] G. Golub and C. Van Loan. Matrix Computations. Johns Hopkins University Press, 1983.

- [15] L. Hagen and A. B. Kahng. Fast spectral methods for ratio cut partitioning and clustering. In *Proc.* ICCAD-91, pages 10-13, 1991. Extended version to appear in IEEE Trans. on CAD, Oct. 1992.
- [16] K. M. Hall. An r-dimensional quadratic placement algorithm. Management Science, 17:219-229, 1970.
- [17] W. R. Heller, C. G. Hsi, and W. F. Mikhail. Wirability-designing wiring space for chips and chip packages. *IEEE Design and Test*, pages 43-51, August 1984.
- [18] W. R. Heller, W. F. Mikhail, and W. E. Donath. Prediction of wiring space requirements for LSI. In *Proc. Design Automation Conf.*, pages 20-22, 1977.
- [19] B. W. Kernighan and S. Lin. An efficient heuristic for partitioning graphs. *Bell Syst. Tech. Jour.*, 49(2):291-307, 1970.
- [20] R. W. Keyes. Fundemental limits in digital information processing. Proceedings of the IEEE, 69:267-278, February 1981.
- [21] S. Kirkpatrick, C. D. Gelatt Jr., and M. P. Vecchi. Optimization by simulated annealing. *Science*, 220(4598):671-680, 1983.
- [22] J. M. Kleinhans, G. Sigl, and F. M. Johannes. Sea-of-gates placement by simultaneous quadratic programming combined with improved partitioning. In *Proc. VLSI89*, 1989.
- [23] R. M. Kling and P. Banerjee. Esp: Placement by simulated evolution. IEEE Transactions on CAD, 8(3):245-256, March 1989.
- [24] B. Krishnamurthy. An improved min-cut algorithm for partitioning VLSI networks. IEEE Transactions on Computers, C-33(5):438-446, 1984.
- [25] F. J. Kurdahi. Area Estimation of VLSI Circuits. PhD thesis, Univ. of So. Calif., 1987.
- [26] F. J. Kurdahi and A. C. Parker. Techniques for area estimation of VLSI layouts. IEEE Transactions on CAD, 8(1):81-92, 1989.
- [27] F. J. Kurdahi and C. Ramachandran. LAST: A layout area and shape function estimator for high level applications. In Proc. Second European Design Automation Conf., February 1991.
- [28] B. Landman and R. Russo. On a pin versus block relationship for partition of logic graphs. IEEE Transactions on Computers, C-20:1469, 1971.
- [29] T. Lengauer. Combinatorial Algorithms for Integrated Circuit Layout. Wiley-Teubner, 1990.

- [30] B. B. Mandelbrot. Fractals: Form, Chance, and Dimension. W. H. Freeman, San Francisco, 1981.
- [31] A. Papoulis. Probability and Statistics. Prentice Hall, 1990.
- [32] R. Russo. On the tradeoff between logic performance and circuit-to-pin ratio for lsi. *IEEE Trans. Computers*, C-21(2):147-152, 1972.
- [33] S. Sastry. Wireability Analysis of Integrated Circuits. PhD thesis, USC, January 1985.
- [34] S. Sastry and A. C. Parker. On the relation between wire length distributions and placement of logic on Master Slice ICs. In *Proc. Design Automation Conf.*, 1984.
- [35] D. G. Schweikert and B. W. Kernighan. A proper model for the partitioning of electrical circuits. In *Proc. Design Automation Conf.*, 1972.
- [36] C. Sechen. Placement and Global Routing of Integrated Circuits Using Simulated Annealing. PhD thesis, Dept, of EECS, Univ. of California, Berkeley, 1986.
- [37] I. E. Sutherland and D. Oestreicher. How big should a printed circuit board be? *IEEE Transactions* on Computers, C-22(5):537-542, May 1973.
- [38] R. S. Tsay and E. S. Kuh. A unified approach to partitioning and placement. In *Princeton Conf. on Inf. and Comp.*, 1986.
- [39] Y. C. Wei and C. K. Cheng. Towards efficient hierarchical designs by ratio cut partitioning. In Proc. ICCAD-89, pages 298-301, 1989.
- [40] Y. C. Wei and C. K. Cheng. Ratio cut partitioning for hierarchical designs. IEEE Transactions on CAD, 10(7):911-921, July 1991.