Computer Science Department Technical Report
Cognitive Systems Laboratory
University of California
Los Angeles, CA 90024-1596

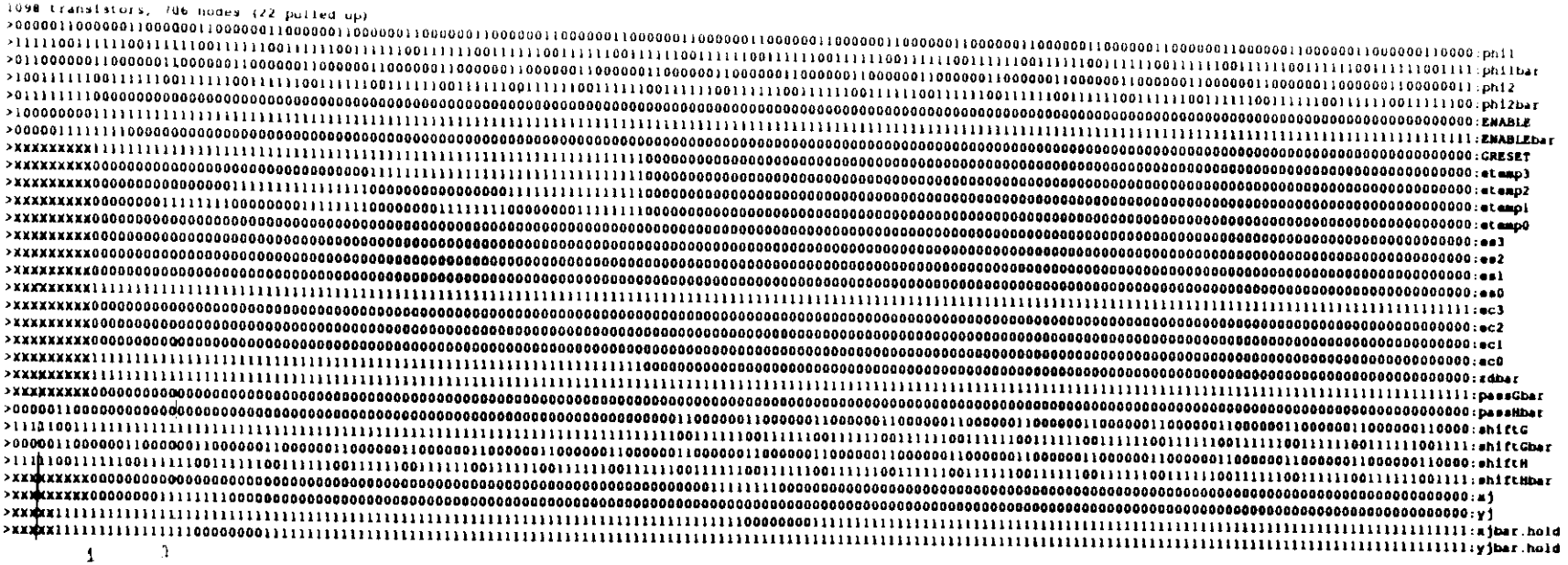
ESIM AND SPICE SIMULATION RESULTS: A VERY LARGE SCALE INTEGRATION DESIGN OF AN ONLINE ALGORITHM FOR THE COMPUTATION OF ROTATION FACTORS

Stephen George Faris

April 1989
CSD-890017

1.1 Esim Results: Individual Units (Cases #1 - #12)

TABLE OF CONTENTS


1098 transistors, 706 nodes (22 pulled up)
ph1l
ph1lbar
ph1r
ph1rbar
ENABLE
ENABLEbar
GRESET
atemp3
atemp2
atemp1
atemp0
as3
as2
as1
as0
ac3
ac2
ac1
ac0
rdbar
passGbar
passHbar
shiftG
shiftGbar
shiftH
shiftHbar
aj
yj
ajbar.hold
yjbar.hold

maui:faris

case1.out

Sat Dec 3 20:42:41 1988

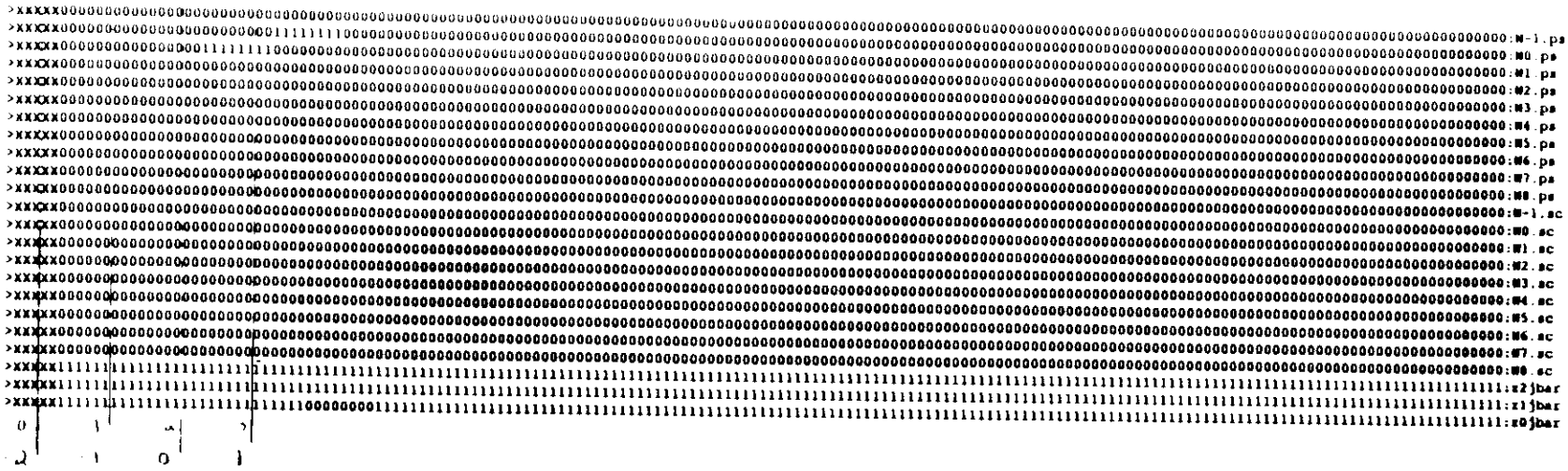
pub3 / Public 3

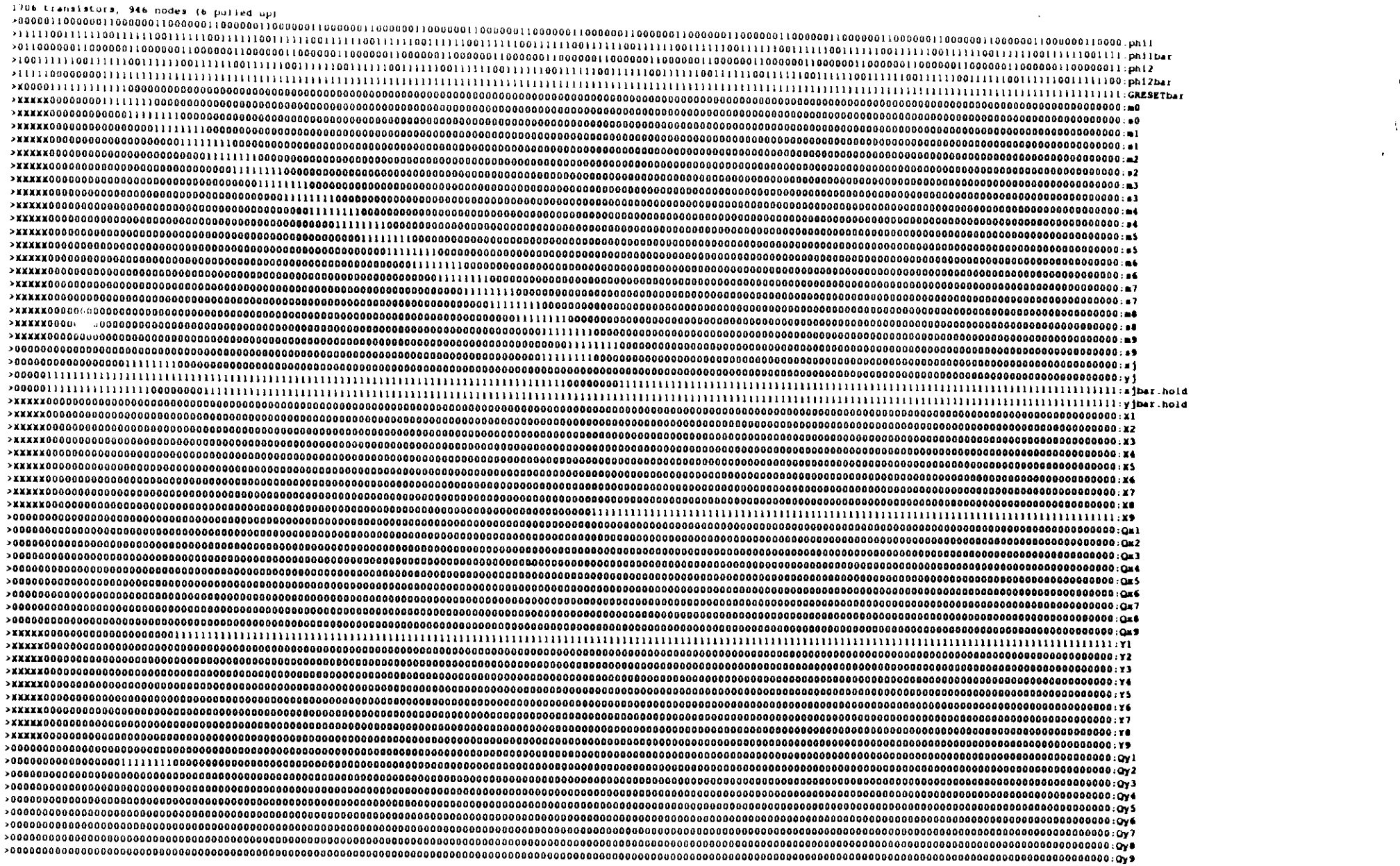
pub3 maui:faris Job: case1.out Date: Sat Dec 3 20:42:41 1988

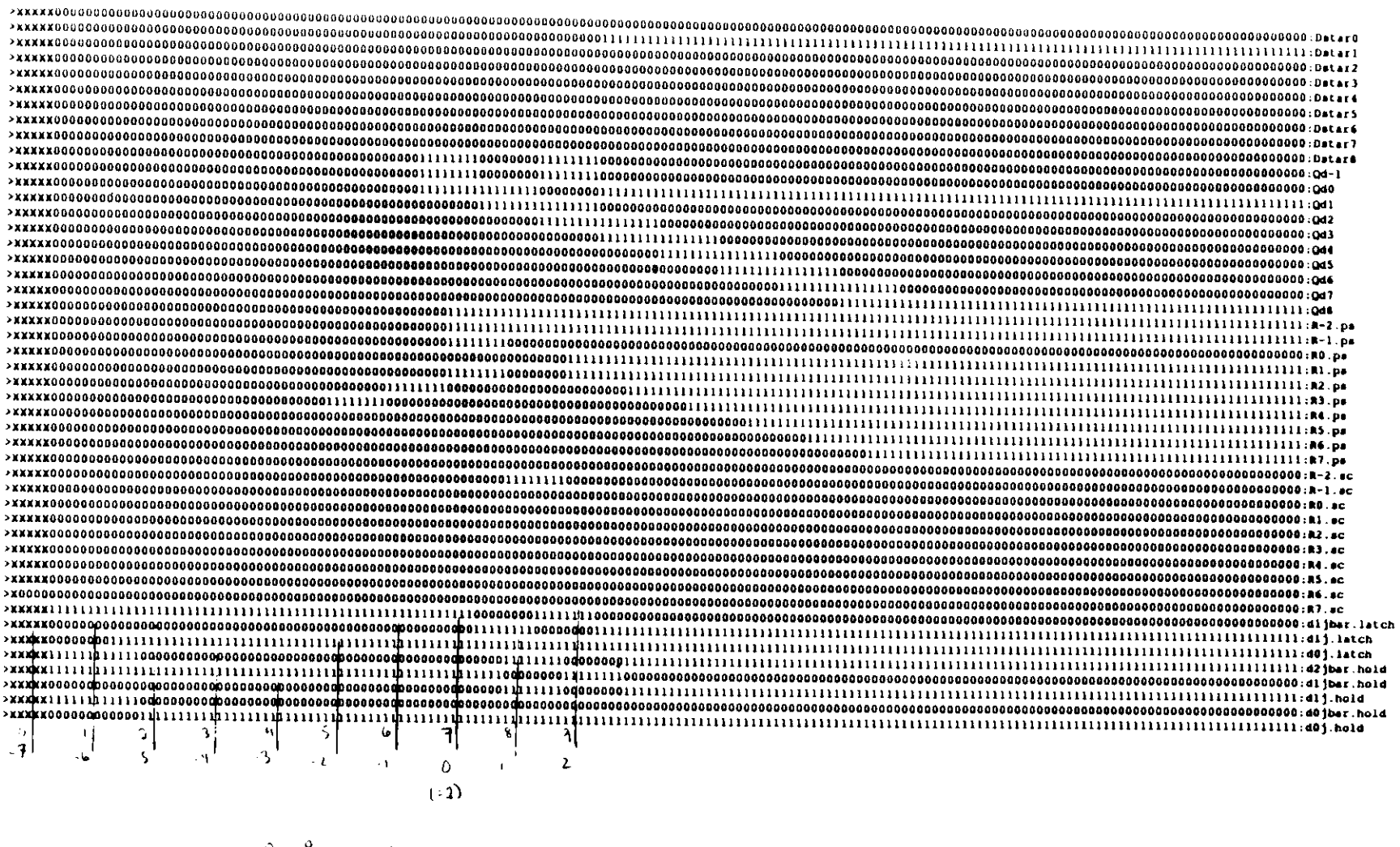
pub3 maui:faris Job: case1.out Date: Sat Dec 3 20:42:41 1988

pub3 maui:faris Job: case1.out Date: Sat Dec 3 20:42:41 1988

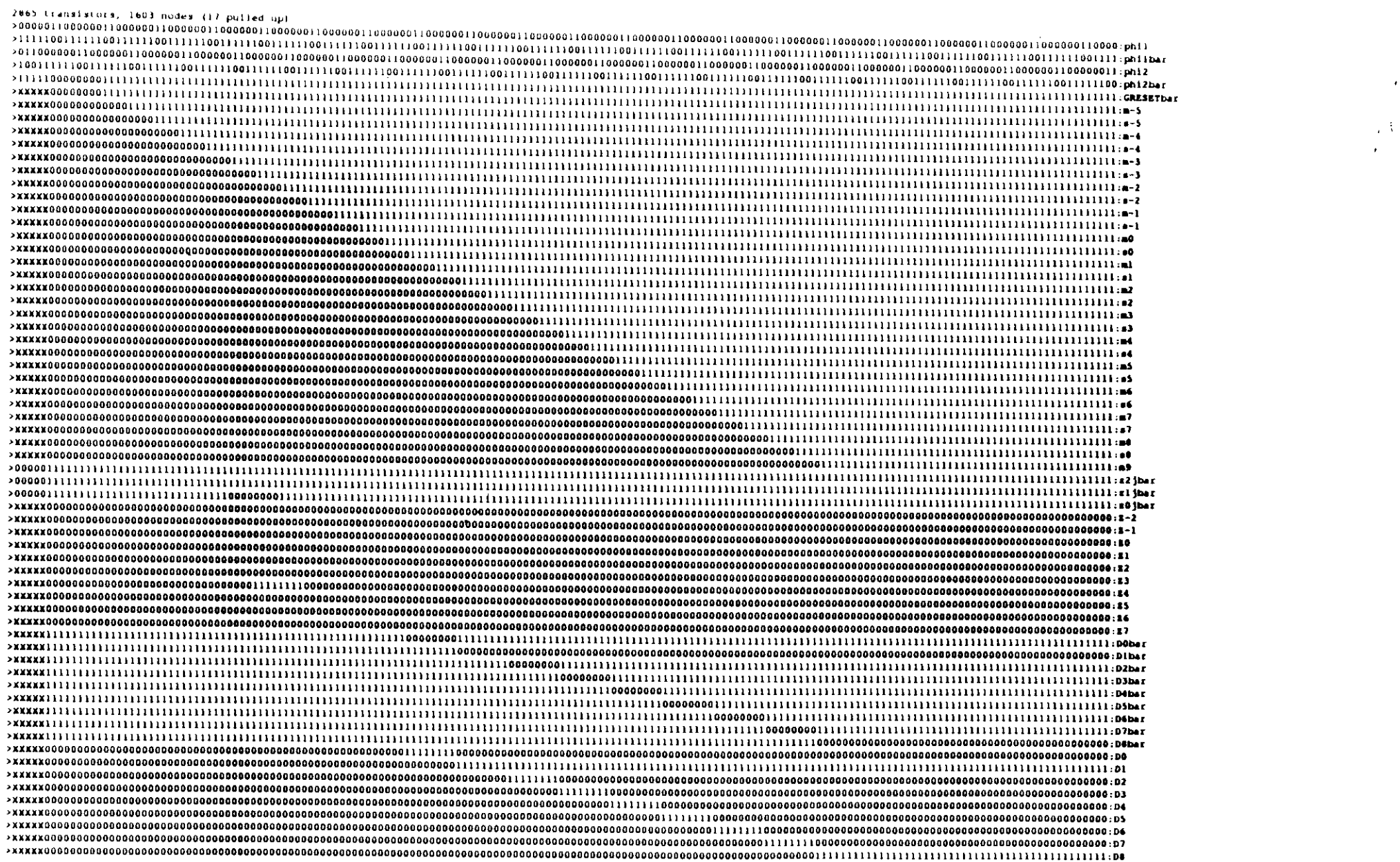
pub3 maui:faris Job: case1.out Date: Sat Dec 3 20:42:41 1988

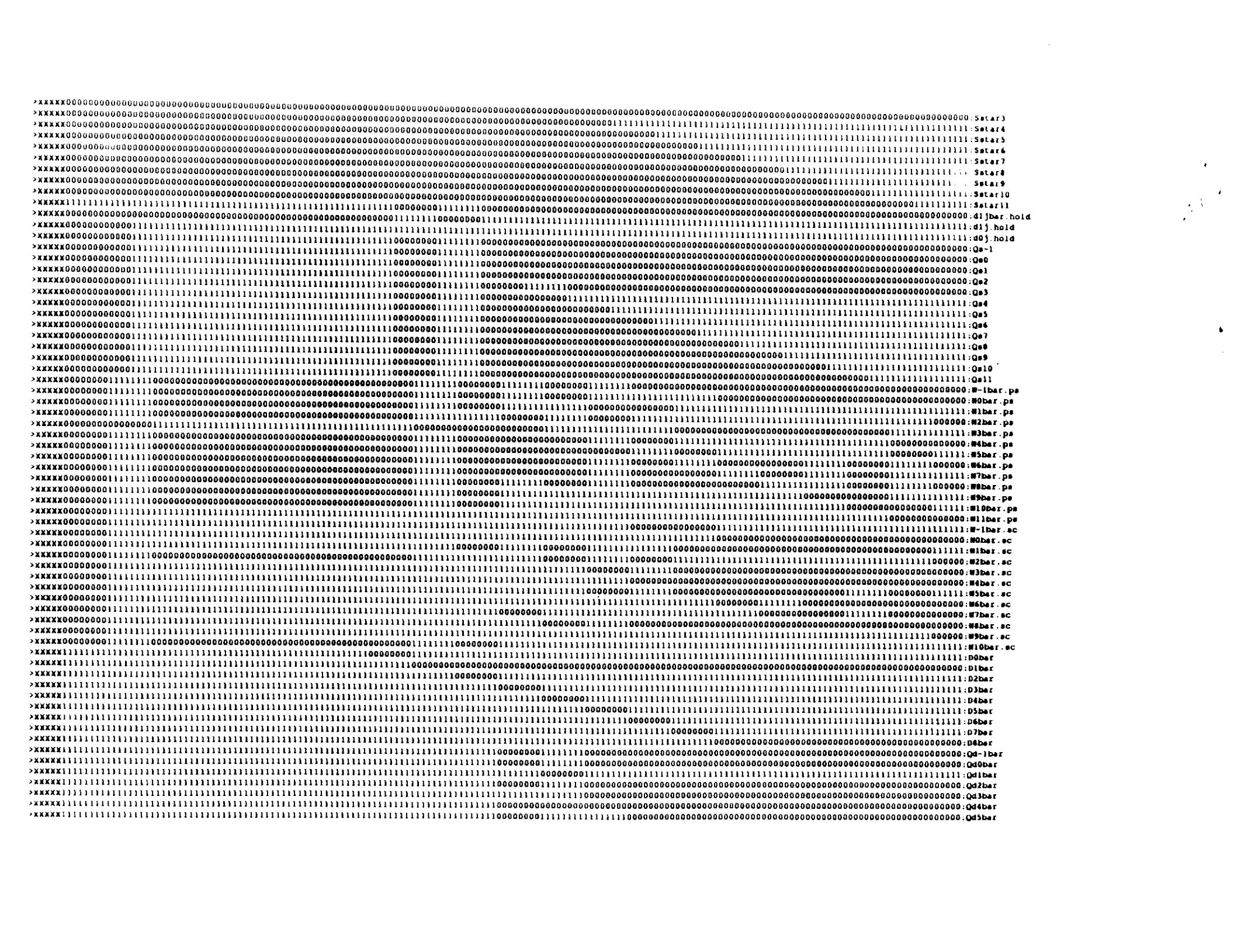

M-1.ps
M0.ps
M1.ps
M2.ps
M3.ps
M4.ps
M5.ps
M6.ps
M7.ps
M8.ps
M-1.sc
M0.sc
M1.sc
M2.sc
M3.sc
M4.sc
M5.sc
M6.sc
M7.sc
M8.sc
x2jbar
x1jbar
x0jbar

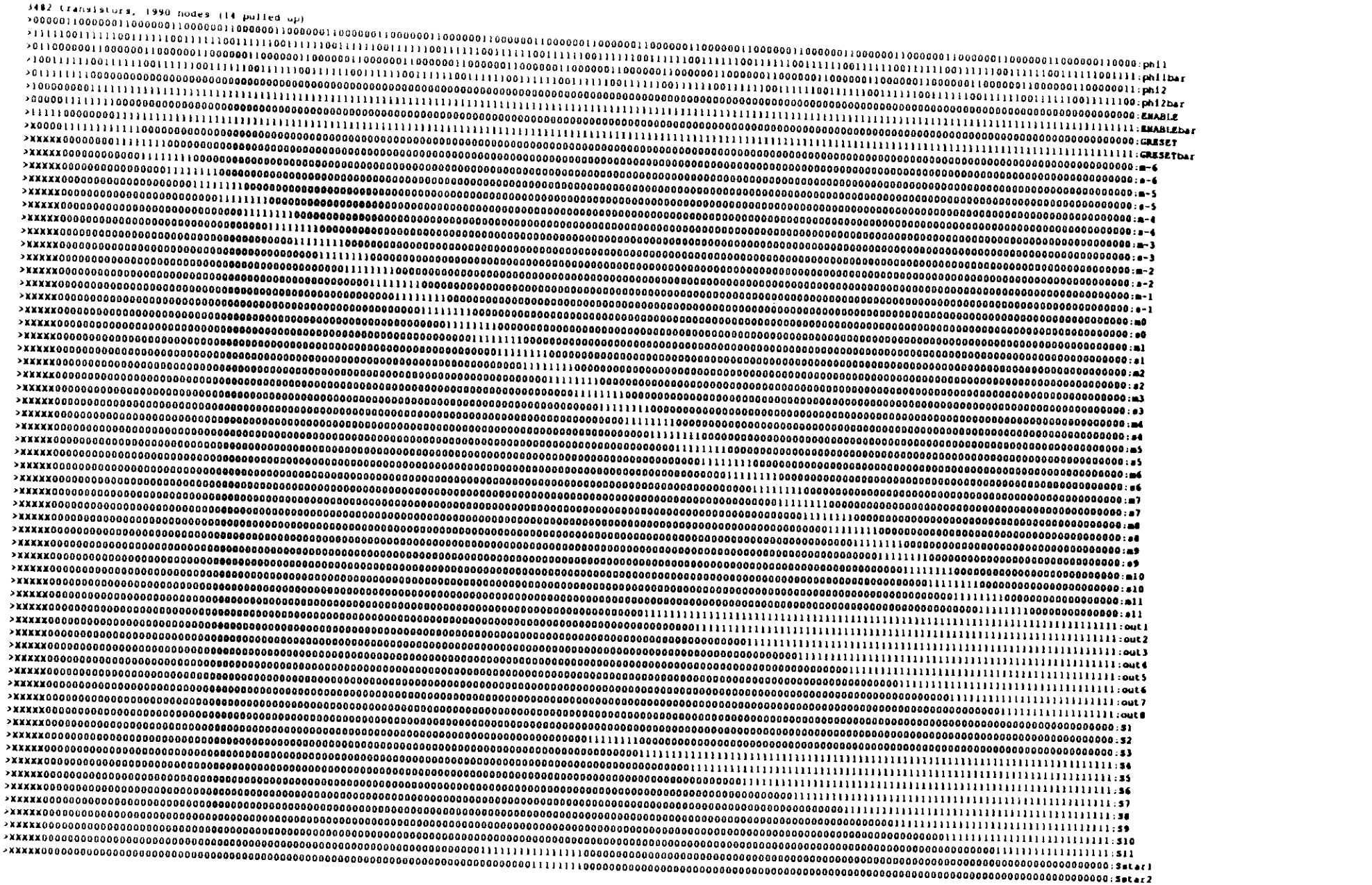

1706 transistors, 946 nodes (6 pulled up)
:ph11
:ph11bar
:ph12
:ph12bar
:GRESETbar
:m0
:s0
:m1
:s1
:m2
:s2
:m3
:s3
:m4
:s4
:m5
:s5
:m6
:s6
:m7
:s7
:m8
:s8
:m9
:s9
:xj
:yj
:xjbar.hold
:yjbar.hold
:X1
:X2
:X3
:X4
:X5
:X6
:X7
:X8
:X9
:Qx1
:Qx2
:Qx3
:Qx4
:Qx5
:Qx6
:Qx7
:Qx8
:Qx9
:Y1
:Y2
:Y3
:Y4
:Y5
:Y6
:Y7
:Y8
:Y9
:Qy1
:Qy2
:Qy3
:Qy4
:Qy5
:Qy6
:Qy7
:Qy8
:Qy9


Datar0
Datar1
Datar2
Datar3
Datar4
Datar5
Datar6
Datar7
Datar8
Qd-1
Qd0
Qd1
Qd2
Qd3
Qd4
Qd5
Qd6
Qd7
Qd8
R-2.ps
R-1.ps
R0.ps
R1.ps
R2.ps
R3.ps
R4.ps
R5.ps
R6.ps
R7.ps
R-2.sc
R-1.sc
R0.sc
R1.sc
R2.sc
R3.sc
R4.sc
R5.sc
R6.sc
R7.sc
d1jbar.latch
d1j.latch
d0j.latch
d2jbar.hold
d1jbar.hold
d1j.hold
d0jbar.hold
d0j.hold
-7
-6
5
-4
-3
-2
-1
0
1
2
(-2)

0..8 usem


2865 transistors, 1603 nodes (17 pulled up)
phi1
phi1bar
phi2
phi2bar
GRESETbar
m-5
s-5
m-4
s-4
m-3
s-3
m-2
s-2
m-1
s-1
m0
s0
m1
s1
m2
s2
m3
s3
m4
s4
m5
s5
m6
s6
m7
s7
m8
s8
m9
s2jbar
s1jbar
s0jbar
E-2
E-1
E0
E1
E2
E3
E4
E5
E6
E7
D0bar
D1bar
D2bar
D3bar
D4bar
D5bar
D6bar
D7bar
D8bar
D0
D1
D2
D3
D4
D5
D6
D7
D8




3482 transistors, 1990 nodes (14 pulled up)
phi1
phi1bar
phi2
phi2bar
ENABLE
ENABLEbar
GRESET
GRESETbar
m-6
s-6
m-5
s-5
m-4
s-4
m-3
s-3
m-2
s-2
m-1
s-1
m0
s0
m1
s1
m2
s2
m3
s3
m4
s4
m5
s5
m6
s6
m7
s7
m8
s8
m9
s9
m10
s10
m11
s11
out1
out2
out3
out4
out5
out6
out7
out8
$1
$2
$3
$4
$5
$6
$7
$8
$9
$10
$11
$star1
$star2

maui:faris

case2.out

Sat Dec 3 21:56:51 1988

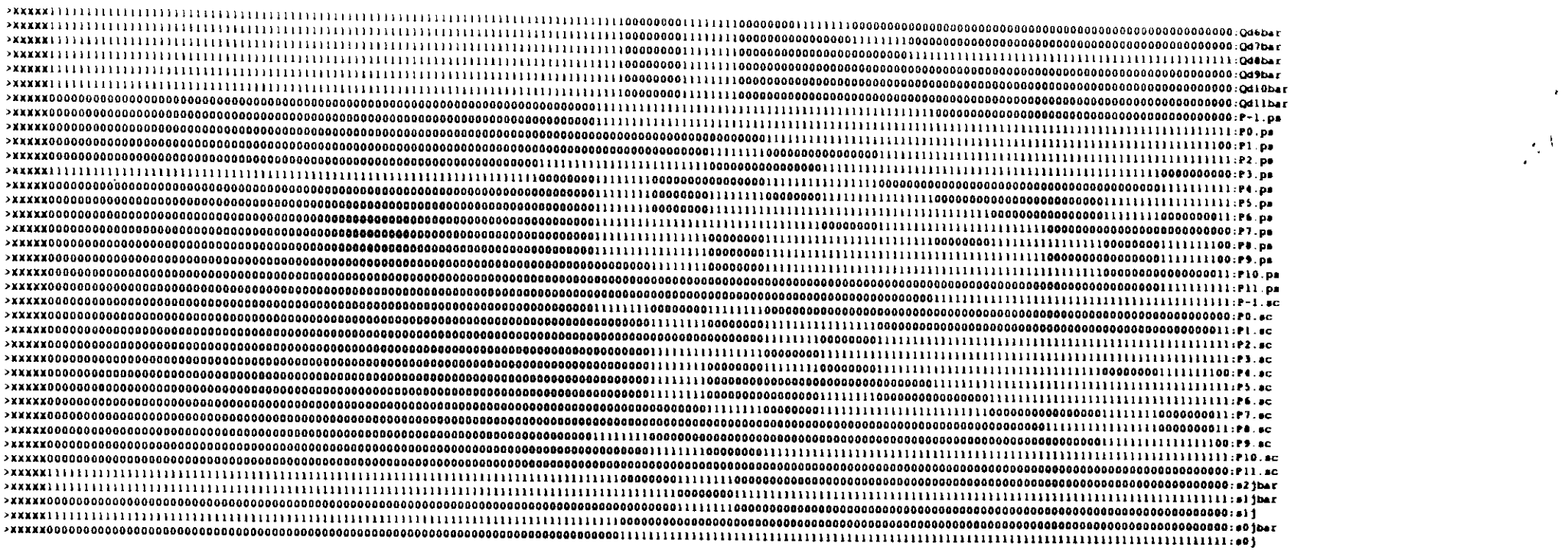
pub3 / Public 3

pub3 maui:faris Job: case2.out Date: Sat Dec 3 21:56:51 1988

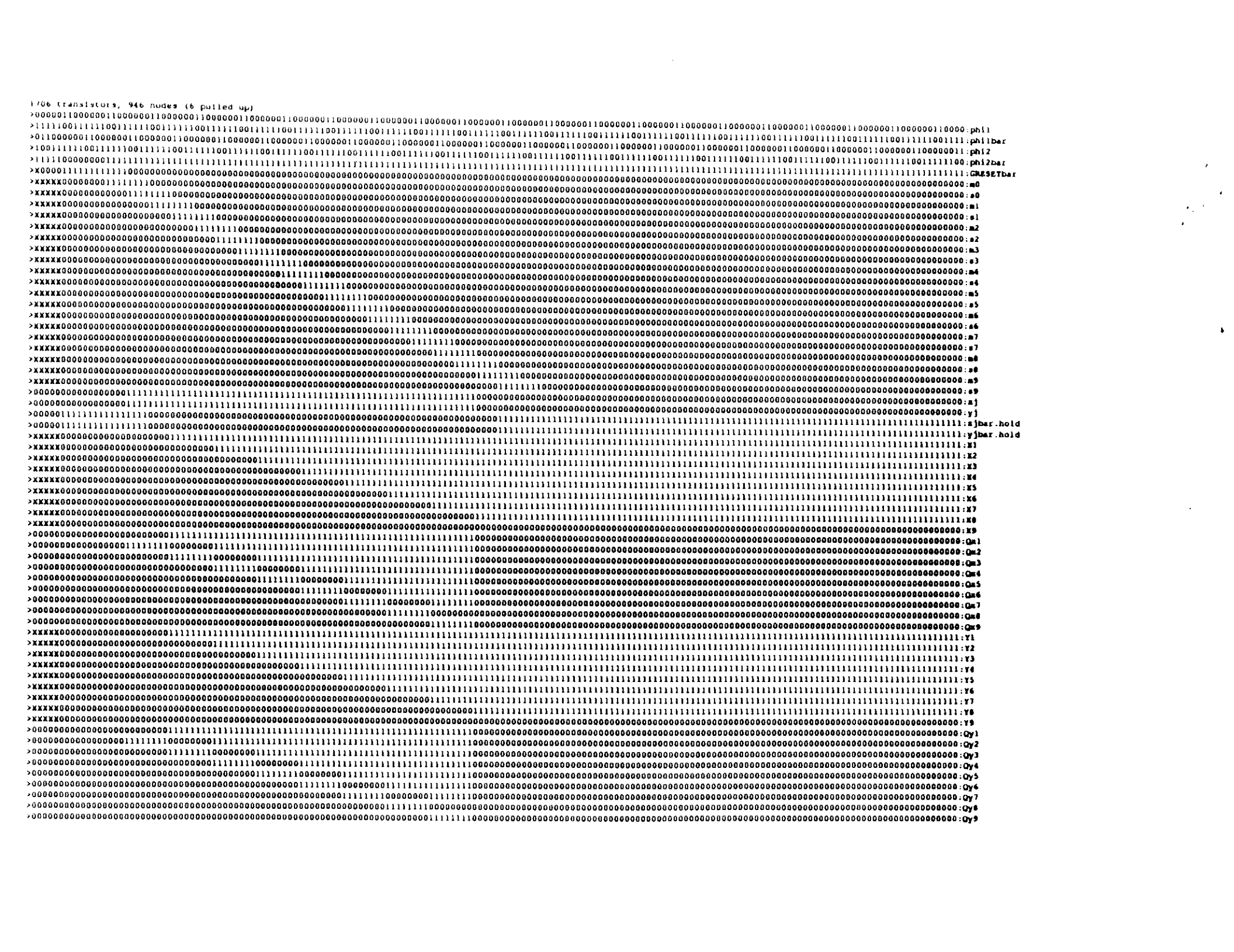
pub3 maui:faris Job: case2.out Date: Sat Dec 3 21:56:51 1988

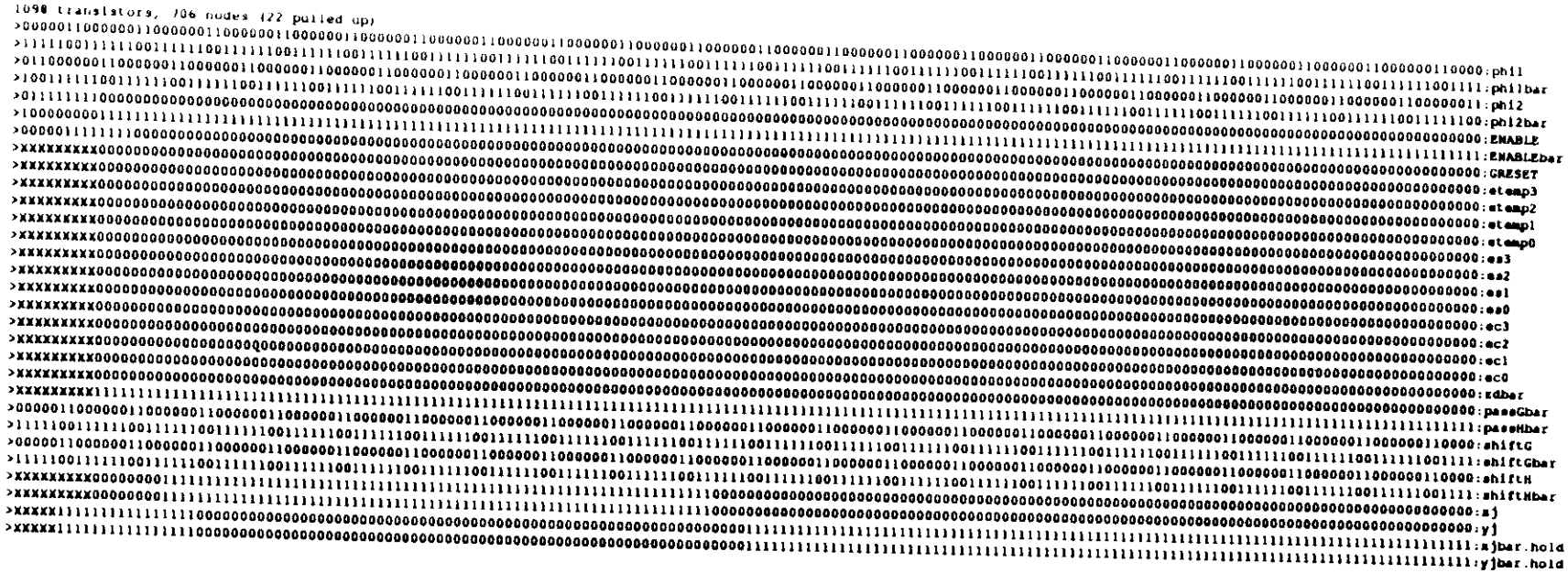
pub3 maui:faris Job: case2.out Date: Sat Dec 3 21:56:51 1988

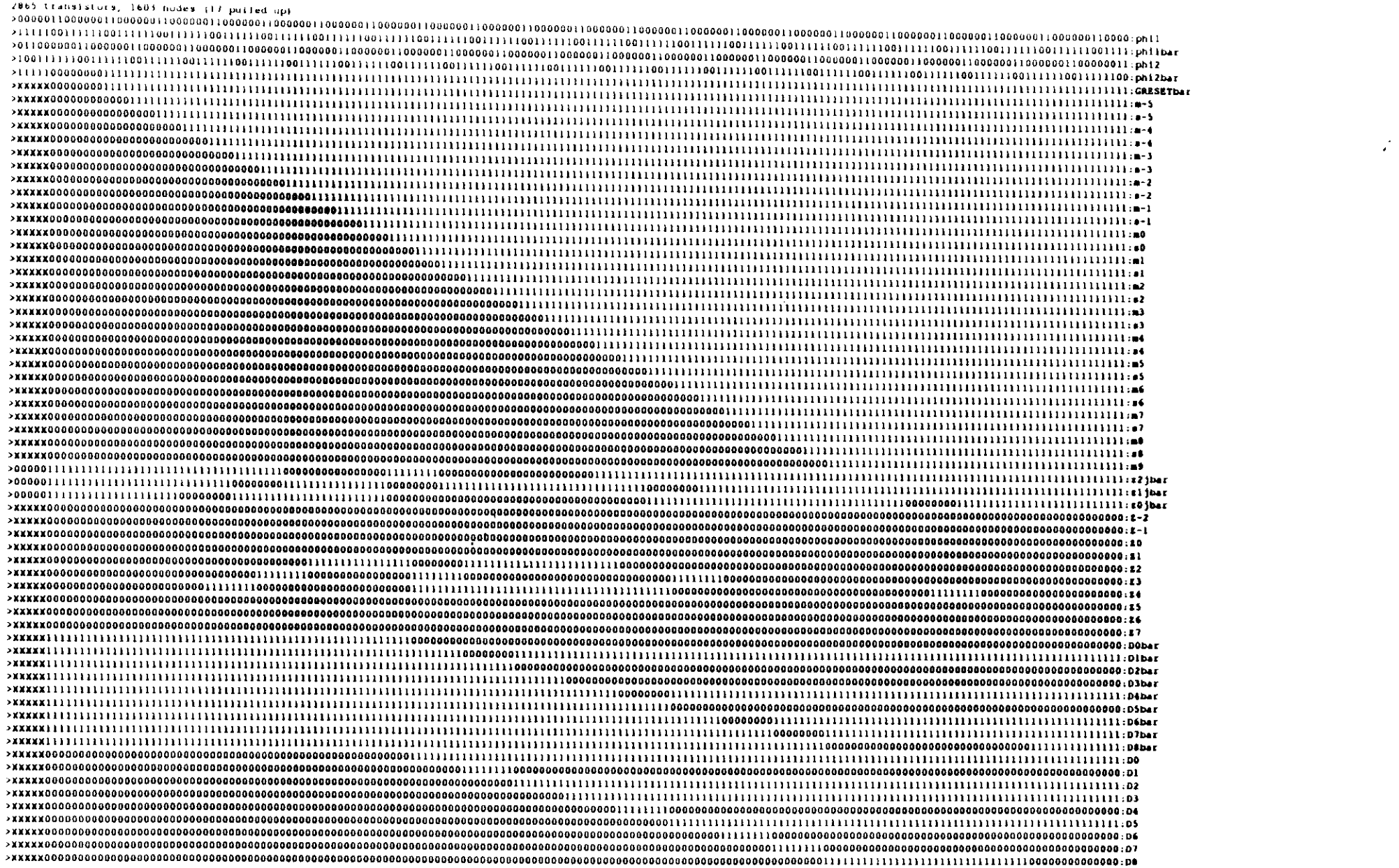
pub3 maui:faris Job: case2.out Date: Sat Dec 3 21:56:51 1988

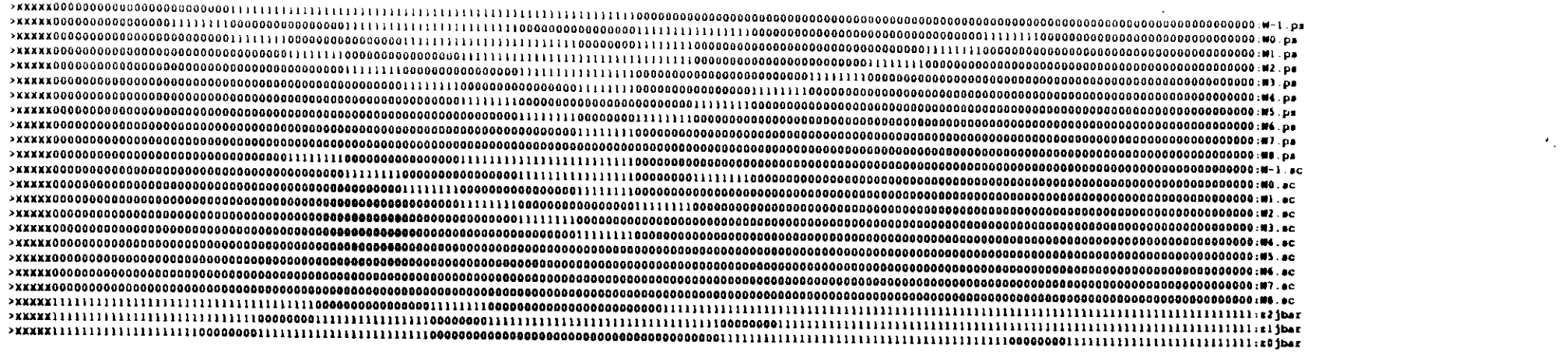


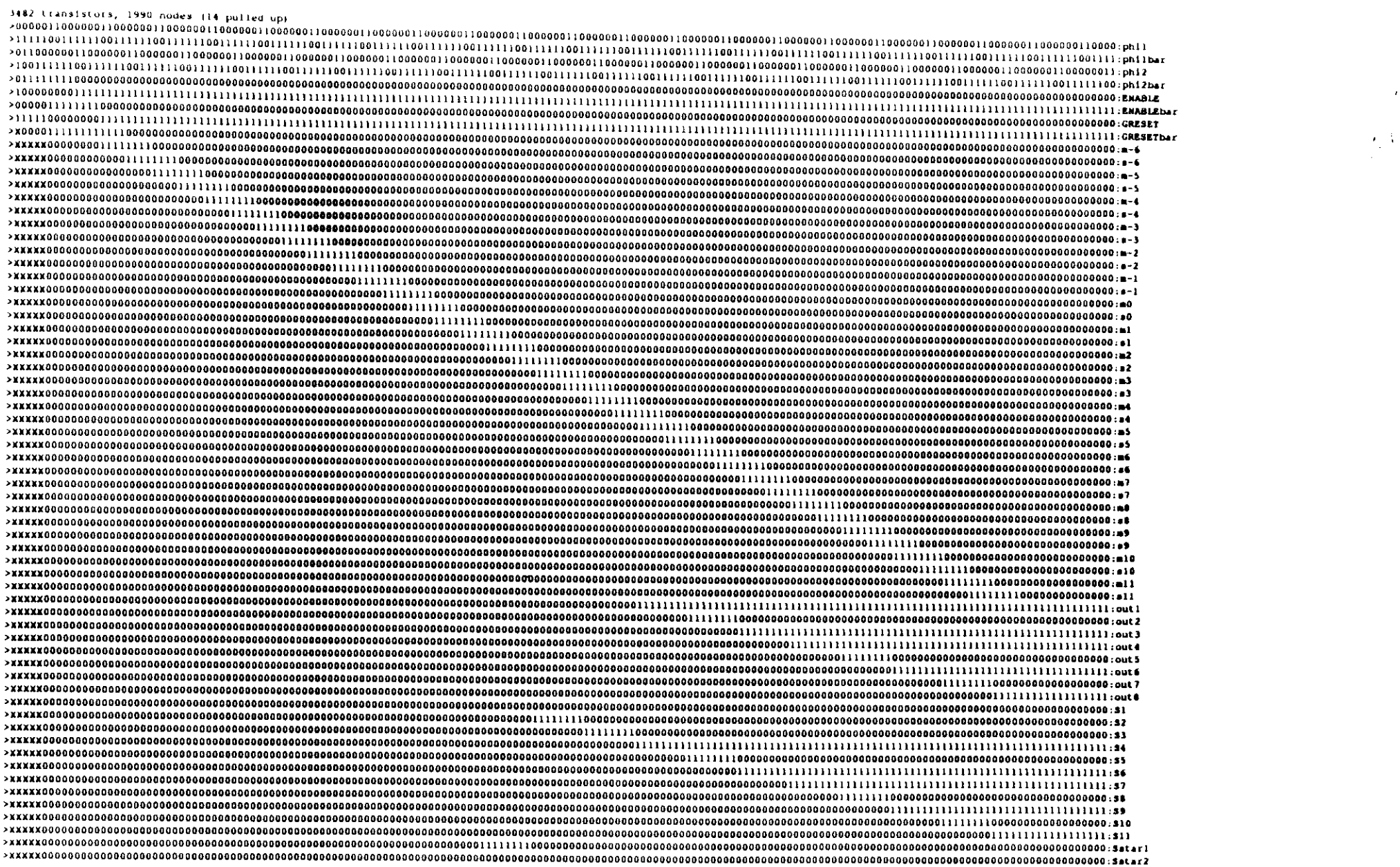
1706 transistors, 946 nodes (6 pulled up)

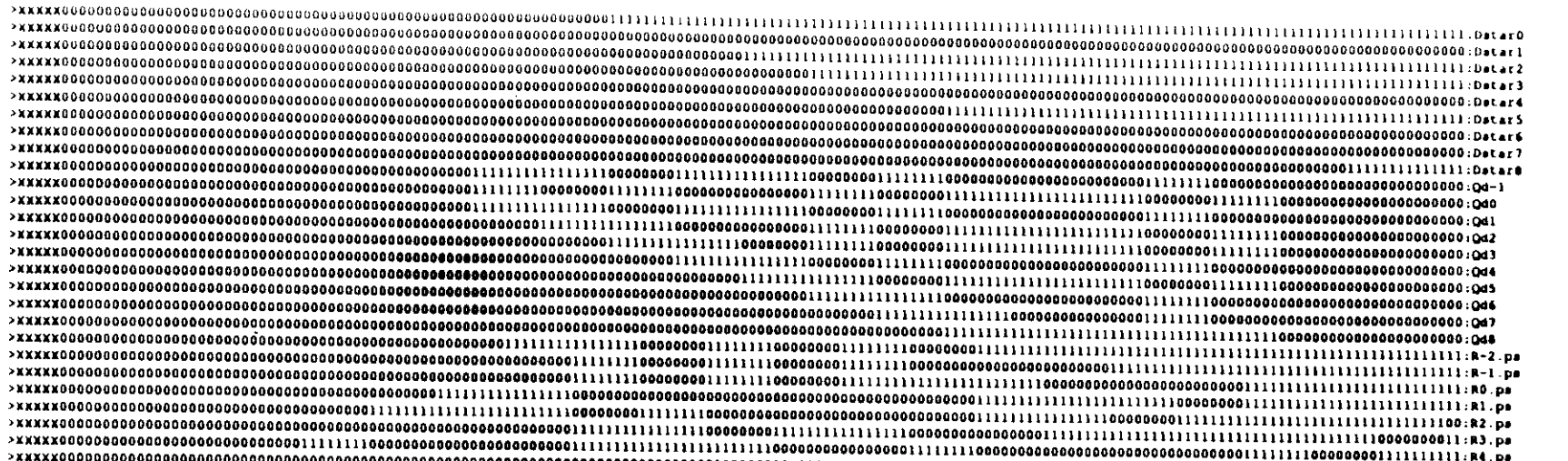


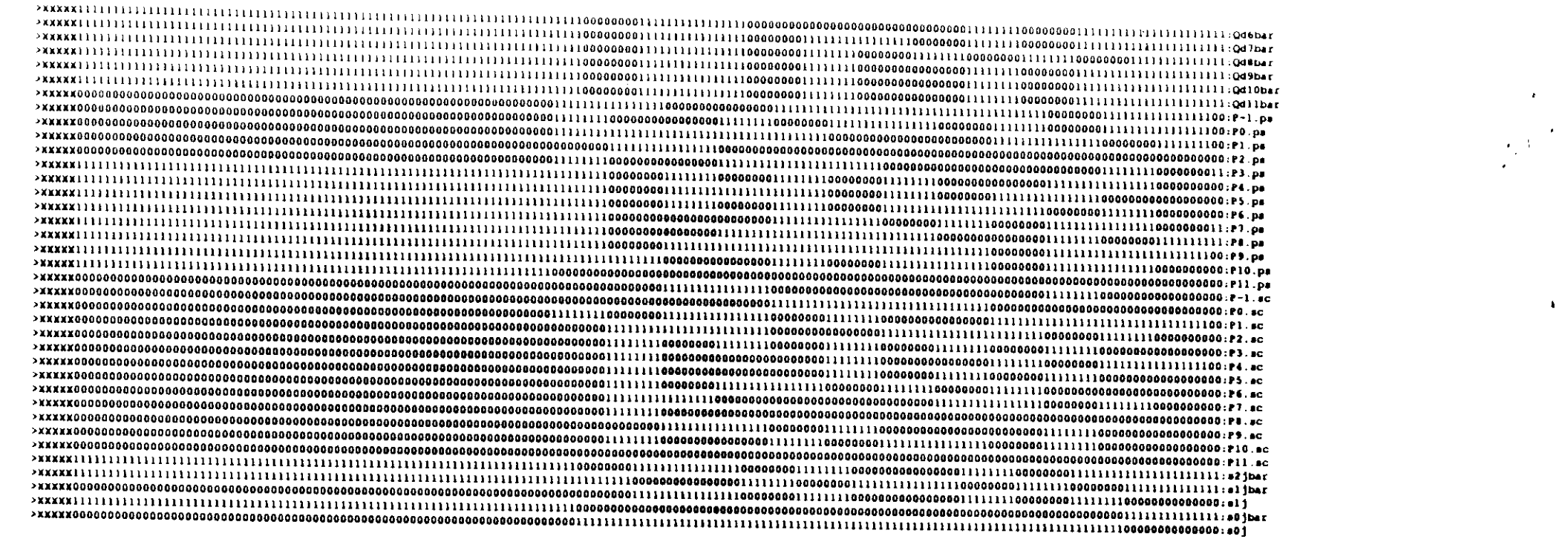

1098 transistors, 706 nodes (22 pulled up)
phi1
phi1bar
phi2
phi2bar
ENABLE
ENABLEbar
GRESET
etemp3
etemp2
etemp1
etemp0
es3
es2
es1
es0
ec3
ec2
ec1
ec0
rdbar
passGbar
passHbar
shiftG
shiftGbar
shiftH
shiftHbar
xj
yj
xjbar.hold
yjbar.hold

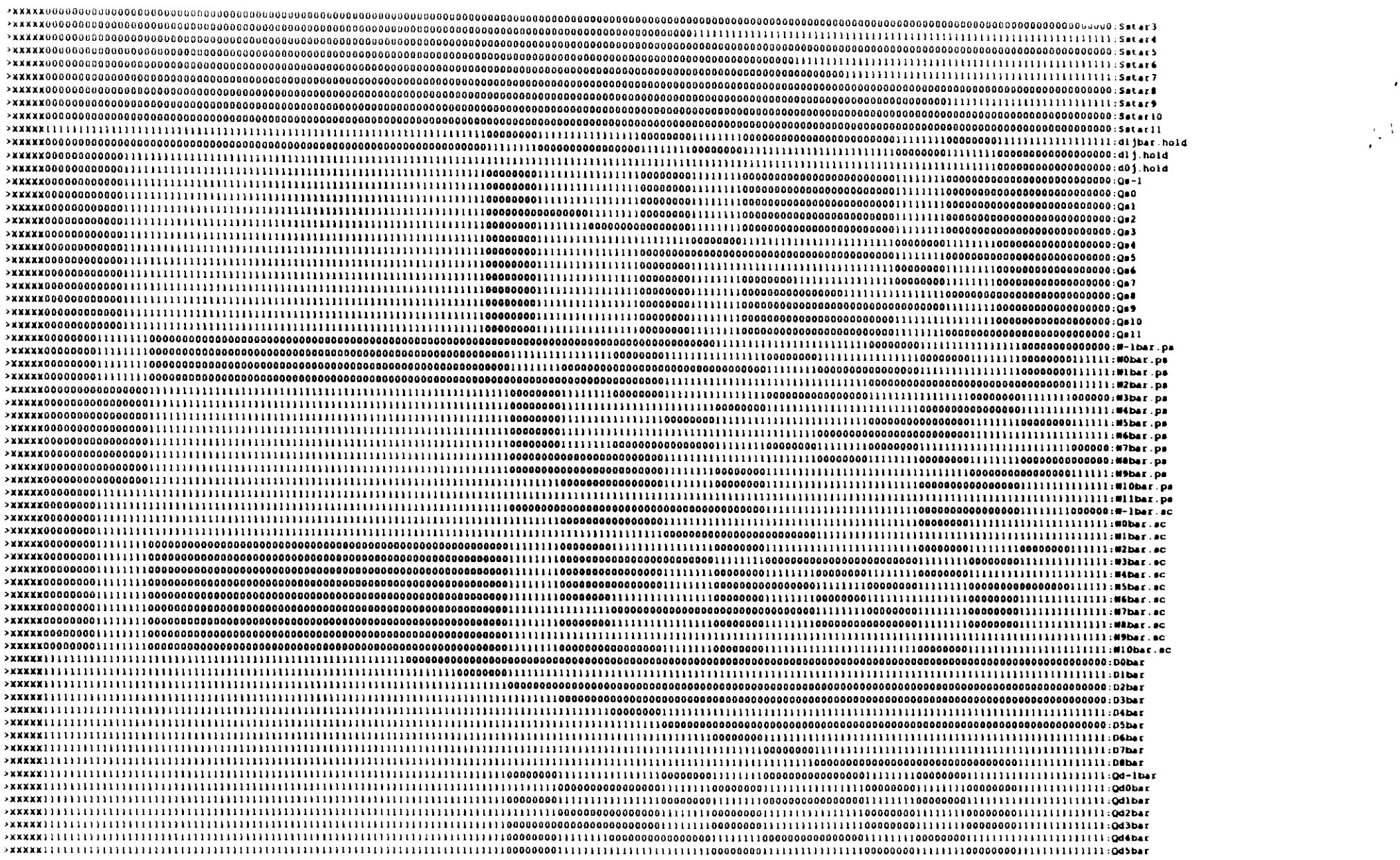

7865 transistors, 1605 nodes (17 pulled up)
phi1
phi1bar
phi2
phi2bar
GRESETbar
m-5
s-5
m-4
s-4
m-3
s-3
m-2
s-2
m-1
s-1
m0
s0
m1
s1
m2
s2
m3
s3
m4
s4
m5
s5
m6
s6
m7
s7
m8
s8
m9
z2jbar
z1jbar
z0jbar
z-2
z-1
z0
z1
z2
z3
z4
z5
z6
z7
D0bar
D1bar
D2bar
D3bar
D4bar
D5bar
D6bar
D7bar
D8bar
D0
D1
D2
D3
D4
D5
D6
D7
D8

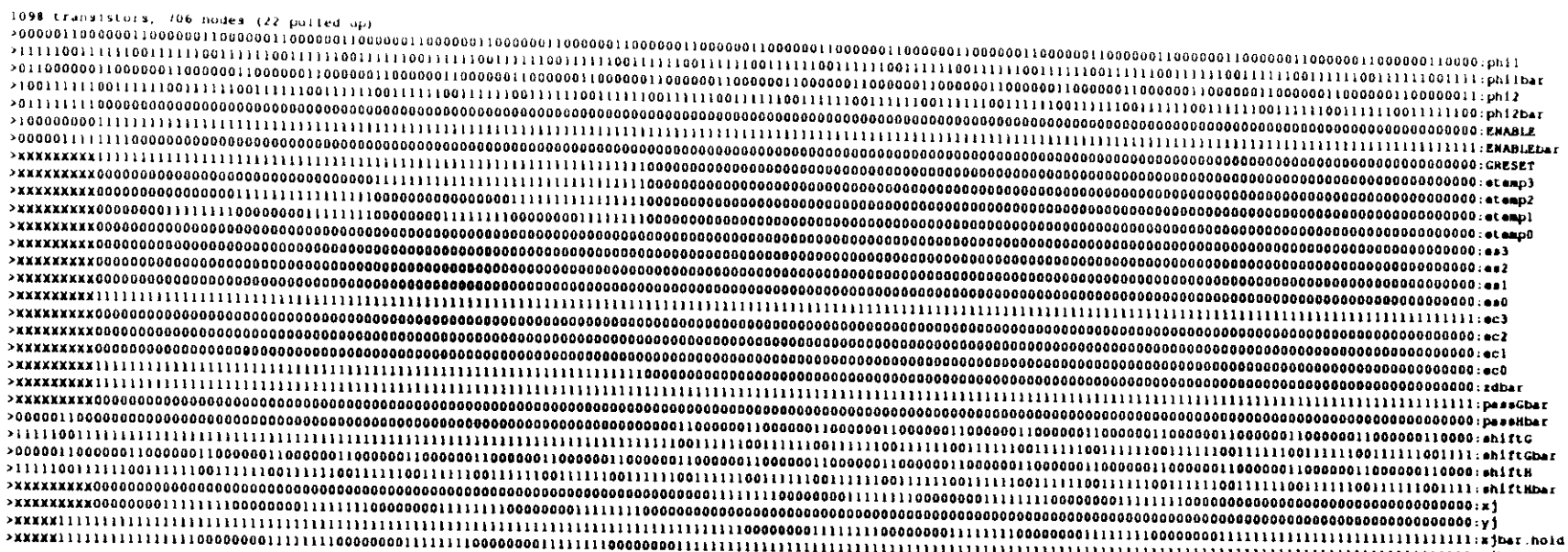

W-1.ps
W0.ps
W1.ps
W2.ps
W3.ps
W4.ps
W5.ps
W6.ps
W7.ps
W8.ps
W-1.sc
W0.sc
W1.sc
W2.sc
W3.sc
W4.sc
W5.sc
W6.sc
W7.sc
W8.sc
z2jbar
z1jbar
z0jbar


3482 transistors, 1990 nodes (14 pulled up)
phi1
phi1bar
phi2
phi2bar
ENABLE
ENABLEbar
GRESET
GRESETbar
m-6
s-6
m-5
s-5
m-4
s-4
m-3
s-3
m-2
s-2
m-1
s-1
m0
s0
m1
s1
m2
s2
m3
s3
m4
s4
m5
s5
m6
s6
m7
s7
m8
s8
m9
s9
m10
s10
m11
s11
out1
out2
out3
out4
out5
out6
out7
out8
$1
$2
$3
$4
$5
$6
$7
$8
$9
$10
$11
$star1
$star2


Dstar0
Dstar1
Dstar2
Dstar3
Dstar4
Dstar5
Dstar6
Dstar7
Dstar8
Qd-1
Qd0
Qd1
Qd2
Qd3
Qd4
Qd5
Qd6
Qd7
Qd8
R-2.ps
R-1.ps
R0.ps
R1.ps
R2.ps
R3.ps
R4.ps
R5.ps
R6.ps
R7.ps
R-2.sc
R-1.sc
R0.sc
R1.sc
R2.sc
R3.sc
R4.sc
R5.sc
R6.sc
R7.sc
dijbar.latch
dij.latch
d0j.latch
d2jbar.hold
dijbar.hold
dij.hold
d0jbar.hold
d0j.hold


Qd6bar
Qd7bar
Qd8bar
Qd9bar
Qd10bar
Qd11bar
P-1.ps
P0.ps
P1.ps
P2.ps
P3.ps
P4.ps
P5.ps
P6.ps
P7.ps
P8.ps
P9.ps
P10.ps
P11.ps
P-1.sc
P0.sc
P1.sc
P2.sc
P3.sc
P4.sc
P5.sc
P6.sc
P7.sc
P8.sc
P9.sc
P10.sc
P11.sc
s2jbar
s1jbar
s1j
s0jbar
s0j




1098 transistors, 706 nodes (22 pulled up)
phi1
phi1bar
phi2
phi2bar
ENABLE
ENABLEbar
GRESET
etemp3
etemp2
etemp1
etemp0
es3
es2
es1
es0
ec3
ec2
ec1
ec0
zdbar
passGbar
passHbar
shiftG
shiftGbar
shiftH
shiftHbar
xj
xjbar.hold
yj
yjbar.hold

maui:faris

case3.out

Sat Dec 3 22:42:10 1988

pub3 / Public 3

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pub3 maui:faris  Job: case3.out  Date: Sat Dec  3 22:42:10 1988

pub3 maui:faris  Job: case3.out  Date: Sat Dec  3 22:42:10 1988

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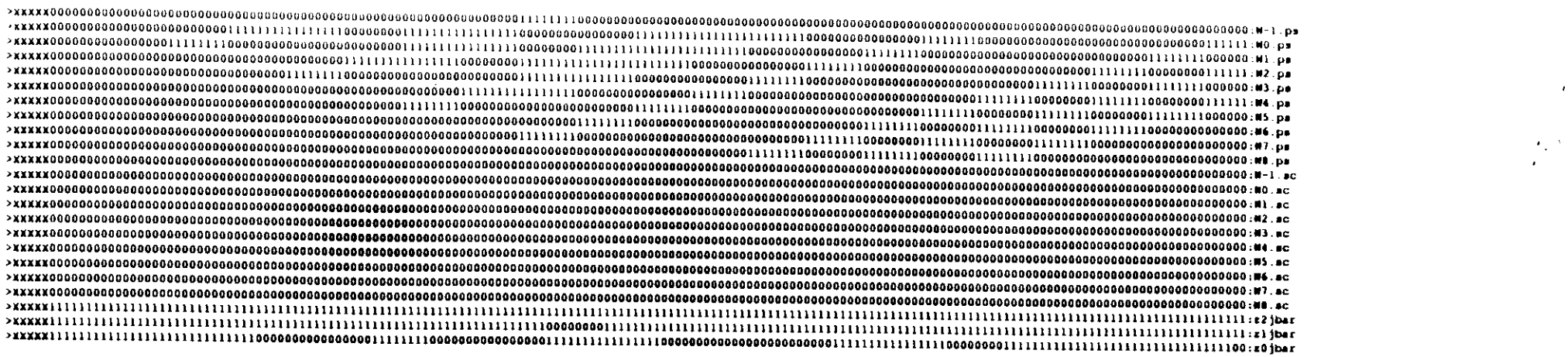
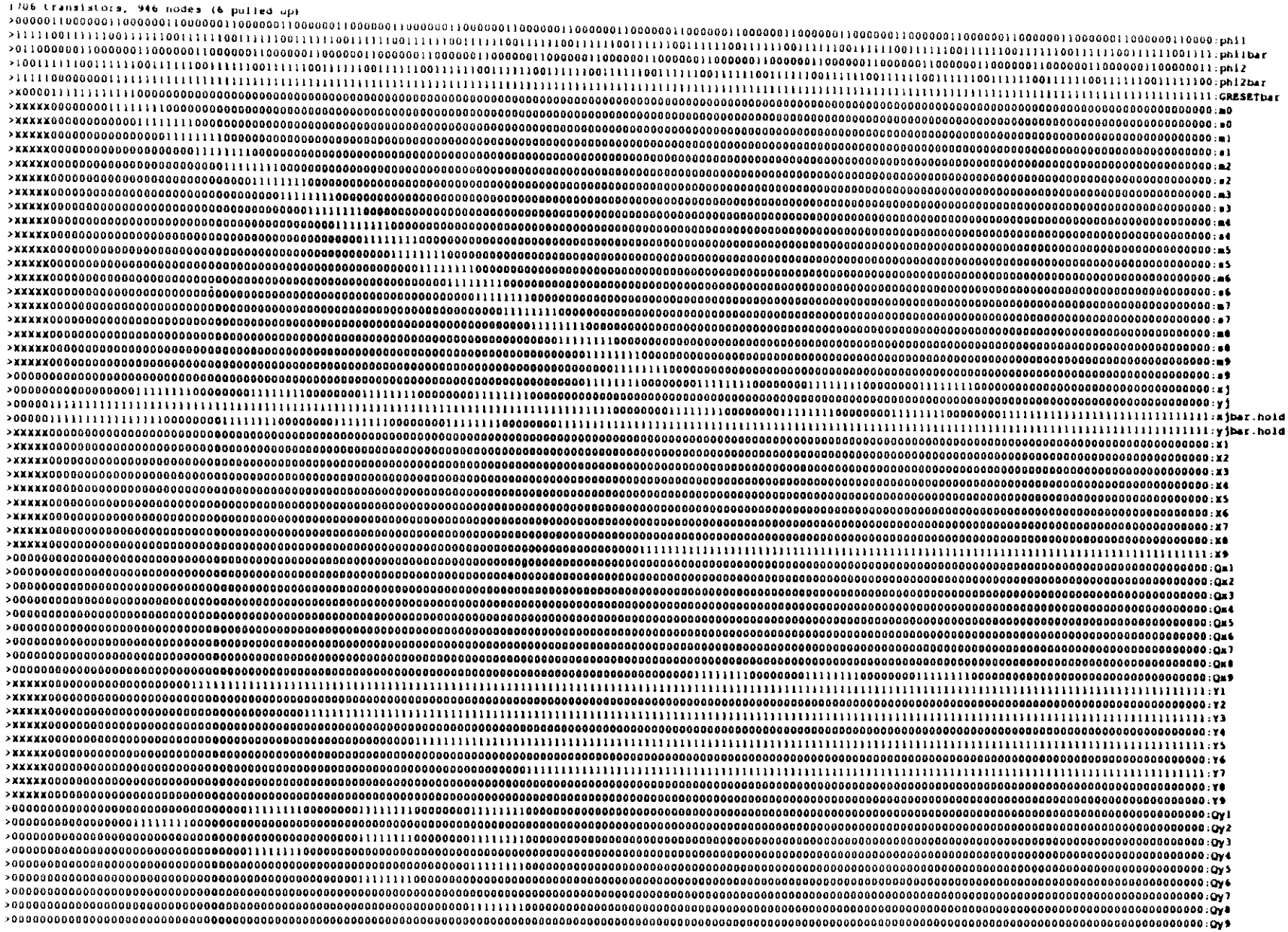
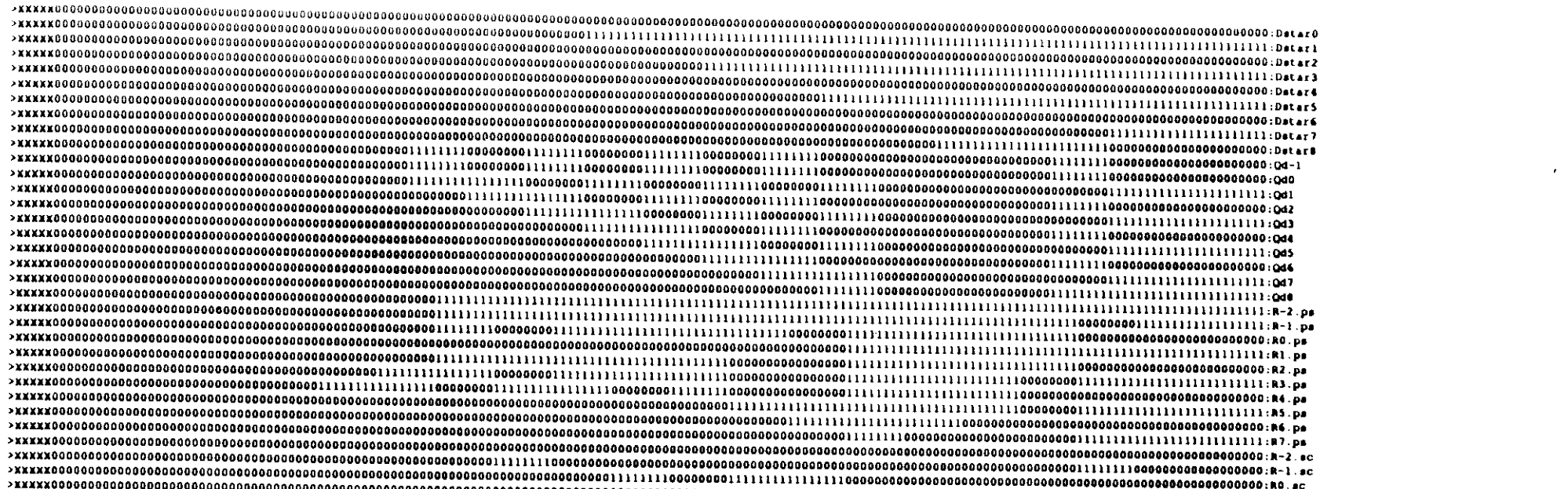
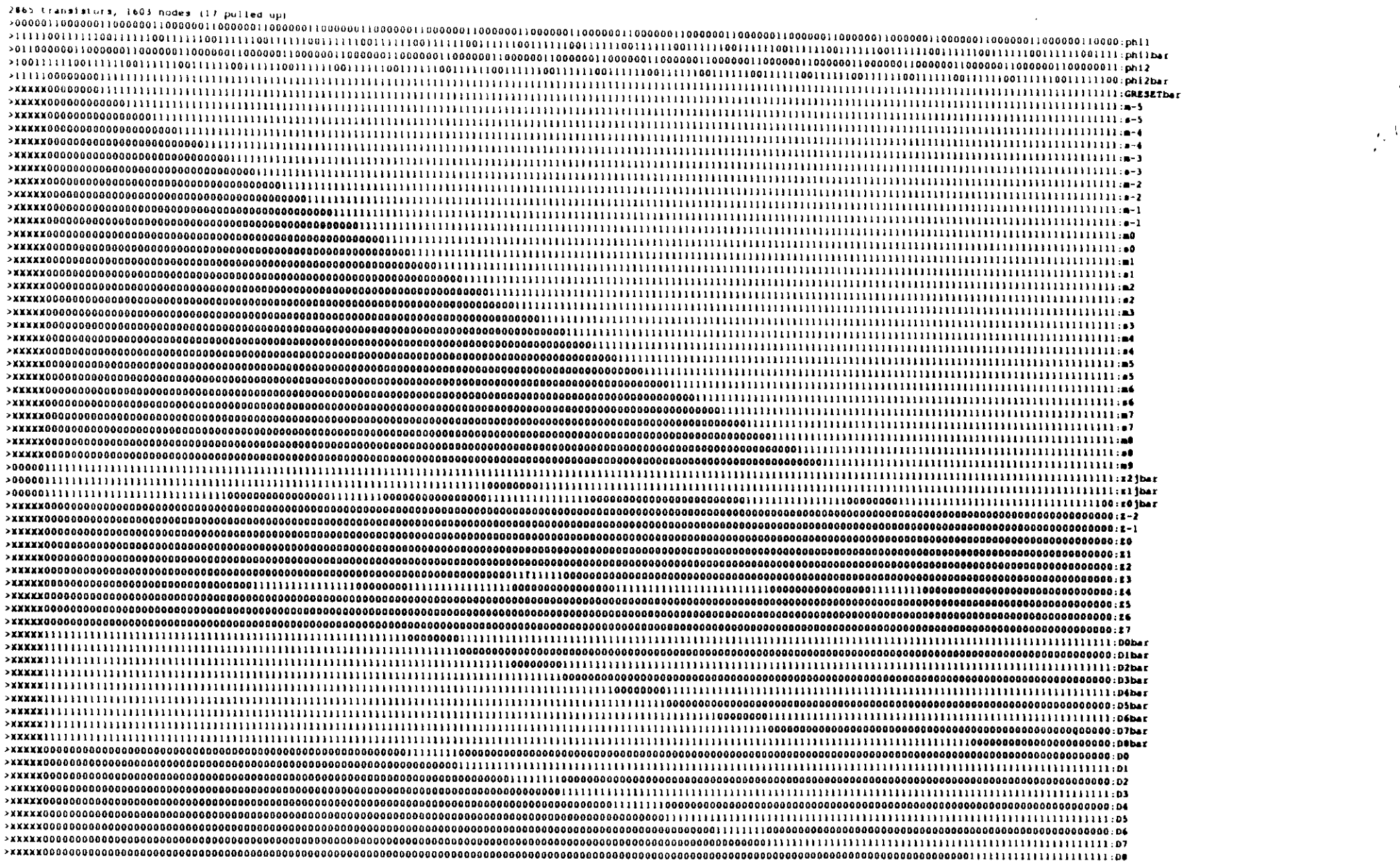
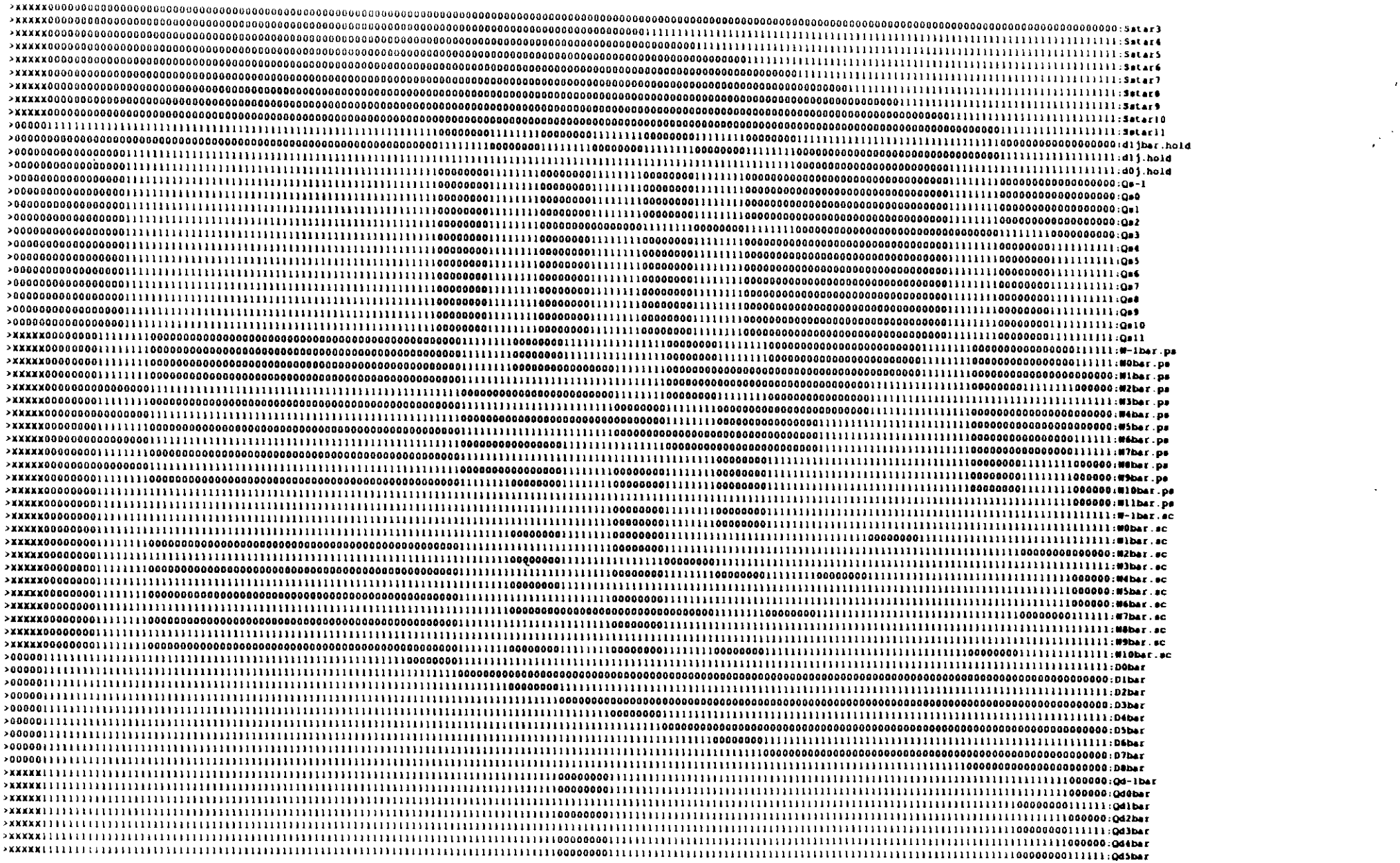

M-1.ps
M0.ps
M1.ps
M2.ps
M3.ps
M4.ps
M5.ps
M6.ps
M7.ps
M8.ps
M-1.ac
M0.ac
M1.ac
M2.ac
M3.ac
M4.ac
M5.ac
M6.ac
M7.ac
M8.ac
z2jbar
z1jbar
z0jbar

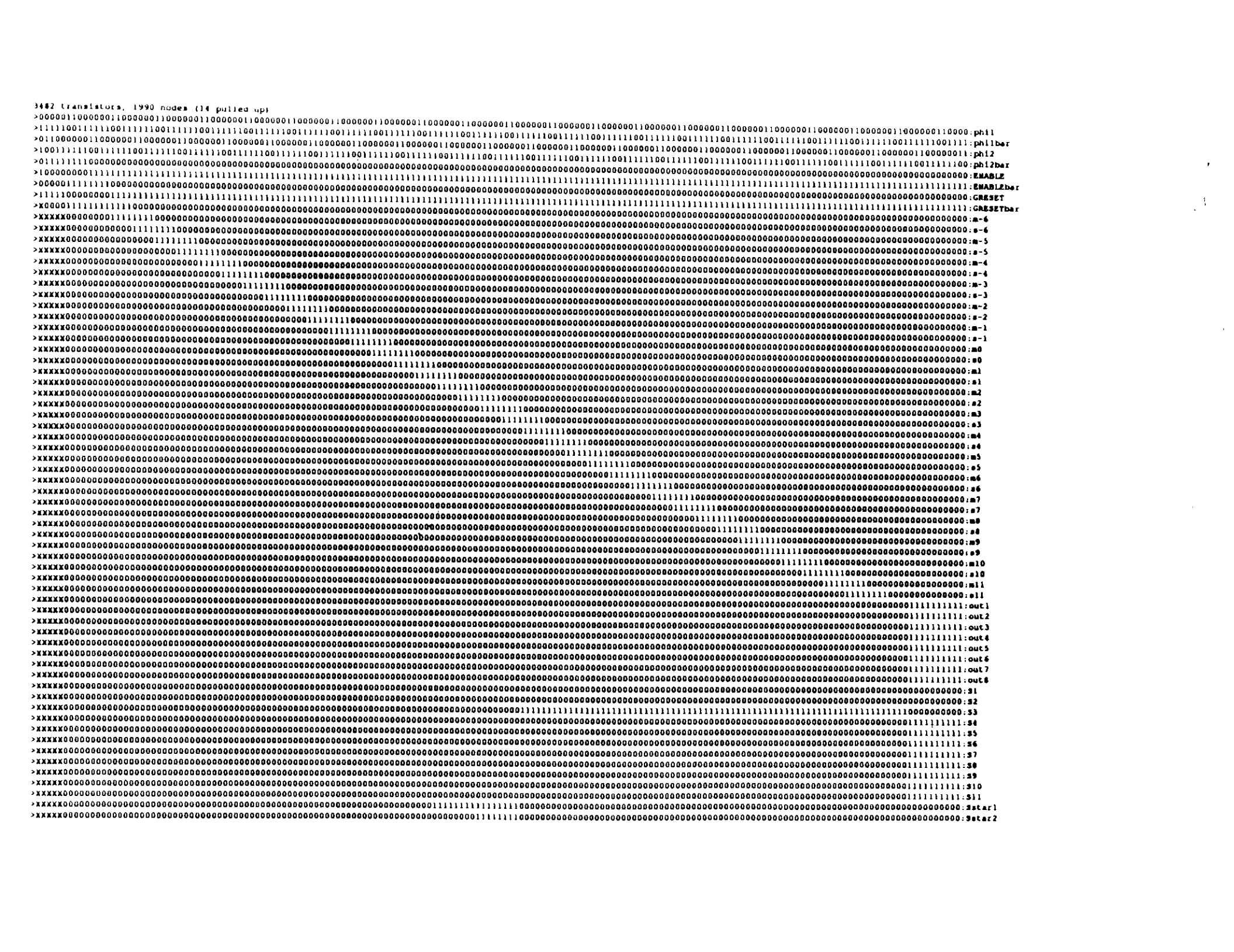
1706 transistors, 946 nodes (6 pulled up)




:Dstar0
:Dstar1
:Dstar2
:Dstar3
:Dstar4
:Dstar5
:Dstar6
:Dstar7
:Dstar8
:Qd-1
:Qd0
:Qd1
:Qd2
:Qd3
:Qd4
:Qd5
:Qd6
:Qd7
:Qd8
:R-2.ps
:R-1.ps
:R0.ps
:R1.ps
:R2.ps
:R3.ps
:R4.ps
:R5.ps
:R6.ps
:R7.ps
:R-2.sc
:R-1.sc
:R0.sc
:R1.sc
:R2.sc
:R3.sc
:R4.sc
:R5.sc
:R6.sc
:R7.sc
:d1jbar.latch
:d1j.latch
:d0j.latch
:d2jbar.hold
:d1jbar.hold
:d1j.hold
:d0jbar.hold
:d0j.hold


2865 transistors, 1603 nodes (17 pulled up)
phi1
phi1bar
phi2
phi2bar
GRESETbar
m-5
s-5
m-4
s-4
m-3
s-3
m-2
s-2
m-1
s-1
m0
s0
m1
s1
m2
s2
m3
s3
m4
s4
m5
s5
m6
s6
m7
s7
m8
s8
m9
x2jbar
x1jbar
r0jbar
Z-2
Z-1
Z0
Z1
Z2
Z3
Z4
Z5
Z6
Z7
D0bar
D1bar
D2bar
D3bar
D4bar
D5bar
D6bar
D7bar
D8bar
D0
D1
D2
D3
D4
D5
D6
D7
D8




3482 translators, 1990 nodes (14 pulled up)
:phi1
:phi1bar
:phi2
:phi2bar
:ENABLE
:ENABLEbar
:GRESET
:GRESETbar
:m-6
:s-6
:m-5
:s-5
:m-4
:s-4
:m-3
:s-3
:m-2
:s-2
:m-1
:s-1
:m0
:s0
:m1
:s1
:m2
:s2
:m3
:s3
:m4
:s4
:m5
:s5
:m6
:s6
:m7
:s7
:m8
:s8
:m9
:s9
:m10
:s10
:m11
:s11
:out1
:out2
:out3
:out4
:out5
:out6
:out7
:out8
:$1
:$2
:$3
:$4
:$5
:$6
:$7
:$8
:$9
:$10
:$11
:$star1
:$star2

maui:faris

case4.out

Sat Dec 3 22:41:36 1988

pub3 / Public 3

pub3 maui:faris Job: case4.out Date: Sat Dec 3 22:41:36 1988

pub3 maui:faris Job: case4.out Date: Sat Dec 3 22:41:36 1988

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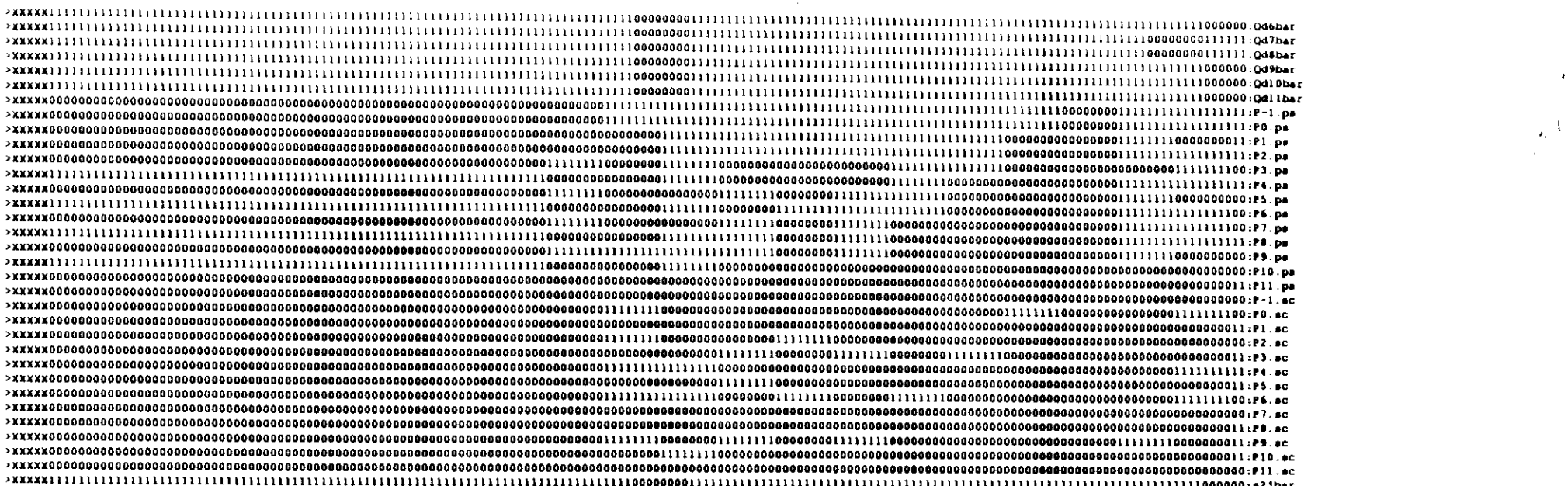
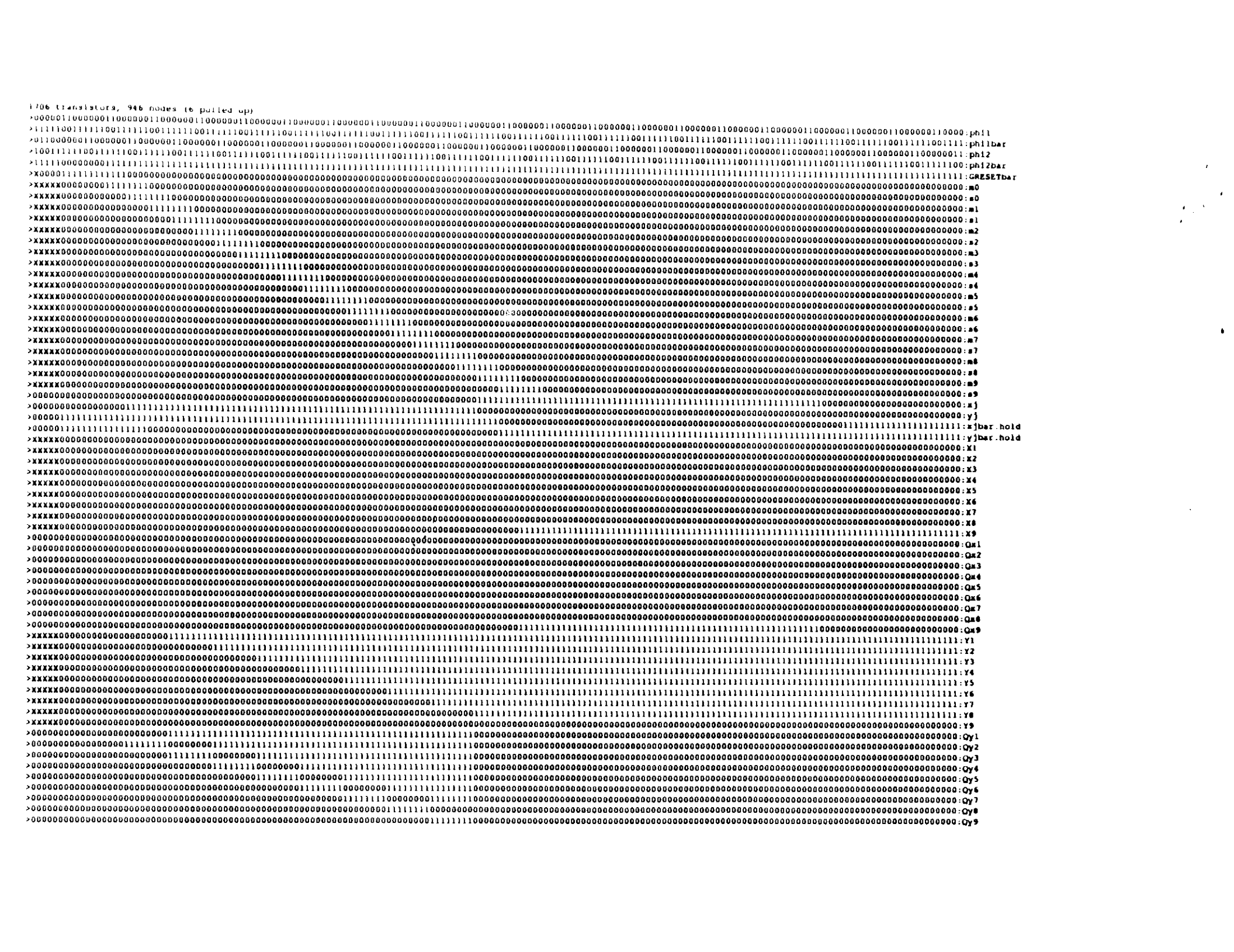
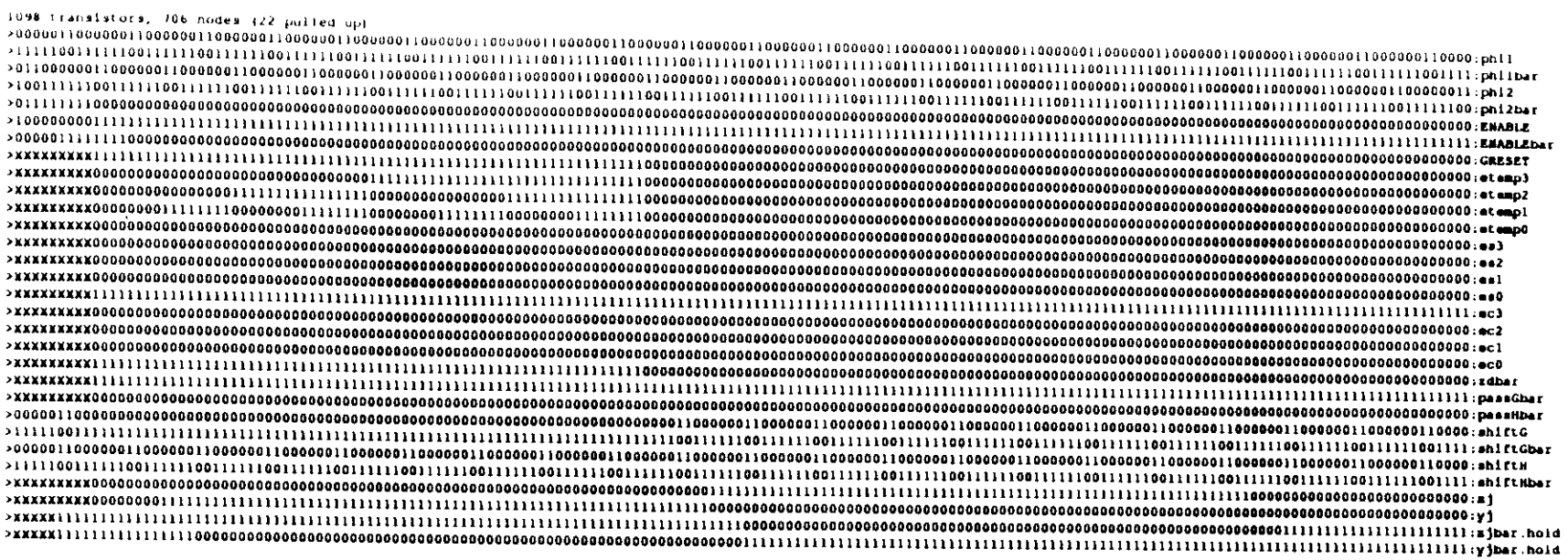
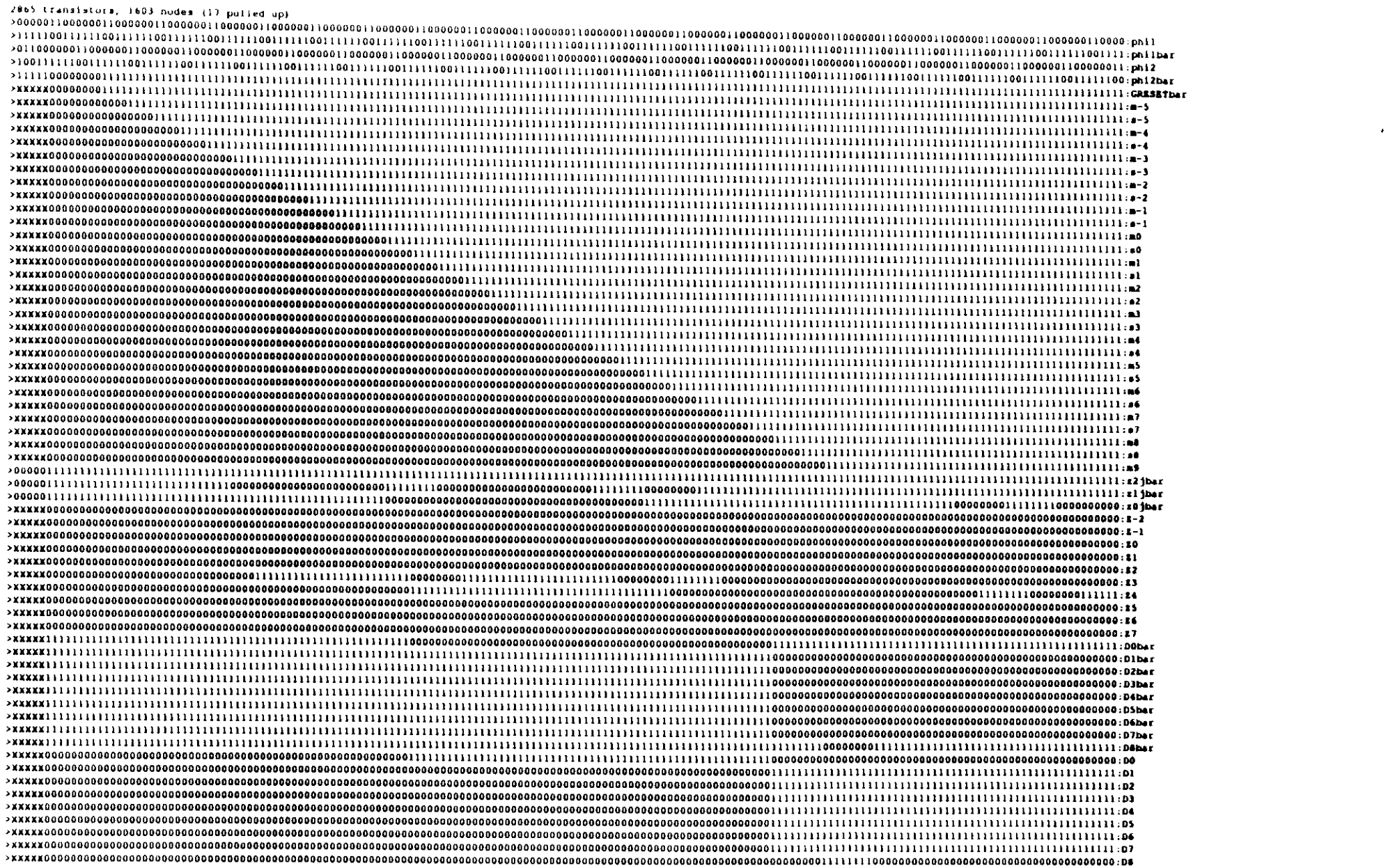
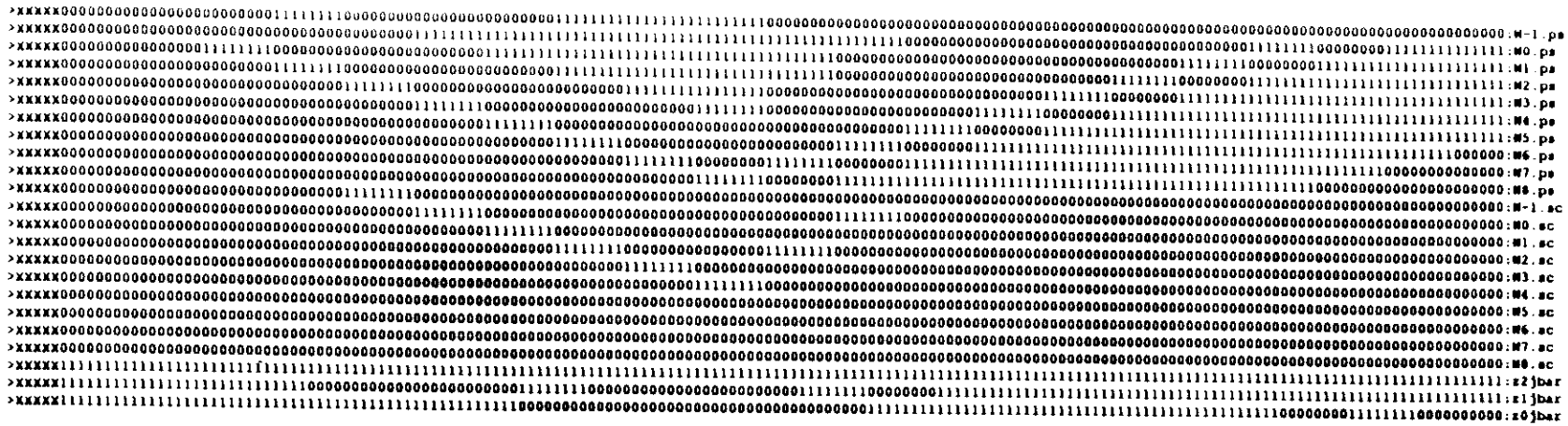
pub3 maui:faris Job: case4.out Date: Sat Dec 3 22:41:36 1988

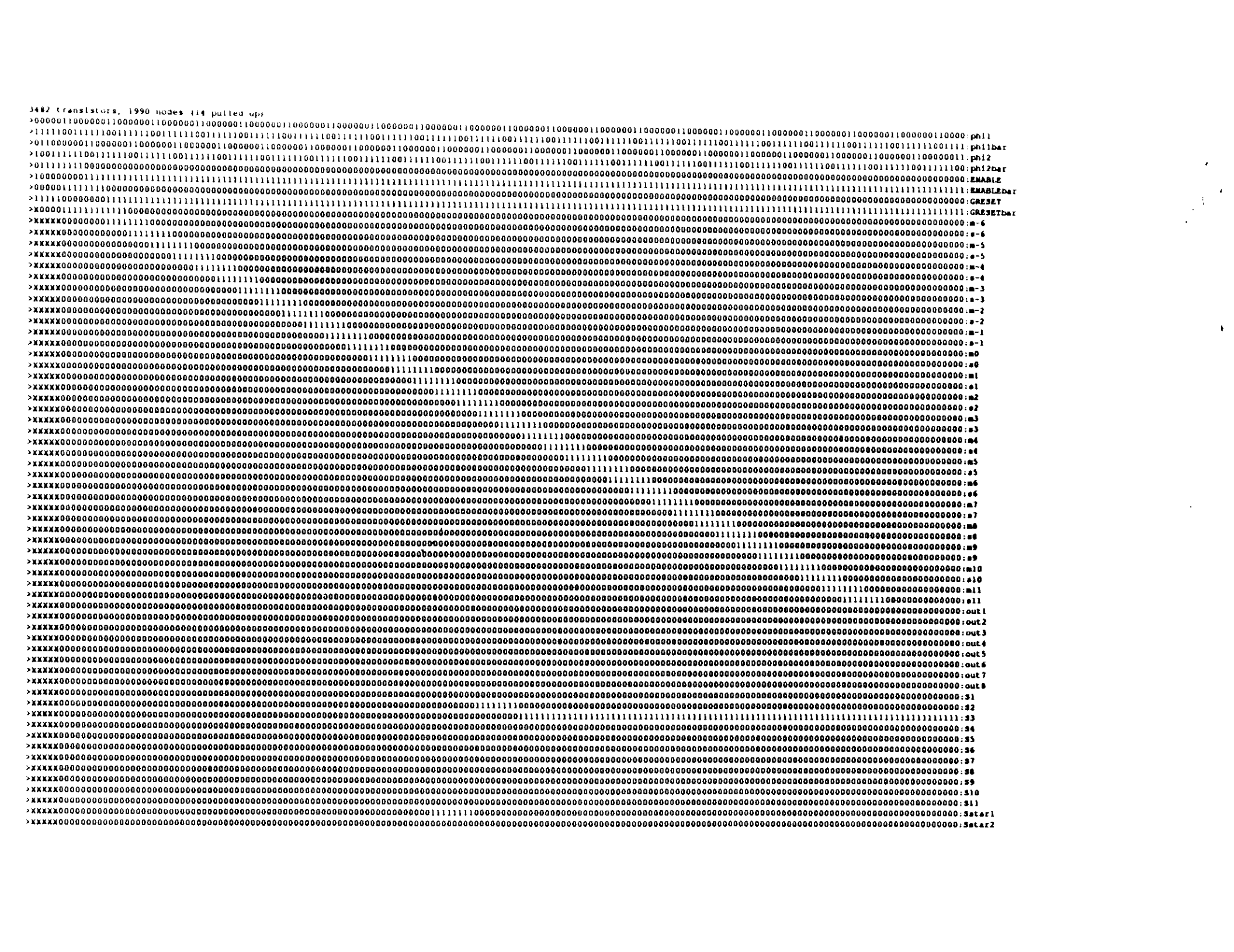


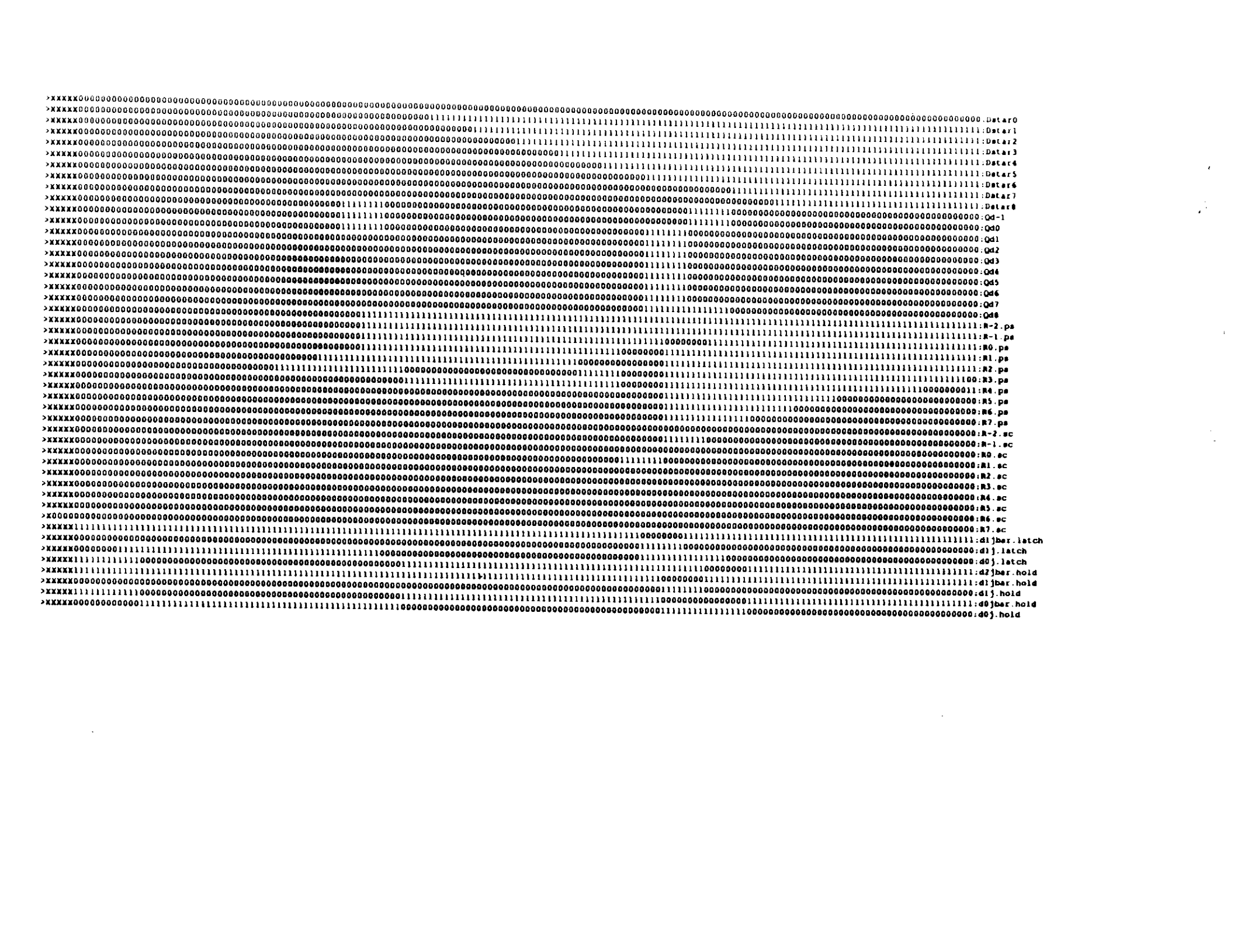

1706 transistors, 946 nodes (6 pulled up)
:ph11
:ph11bar
:ph12
:ph12bar
:GRESETbar
:m0
:s0
:m1
:s1
:m2
:s2
:m3
:s3
:m4
:s4
:m5
:s5
:m6
:s6
:m7
:s7
:m8
:s8
:m9
:s9
:xj
:yj
:xjbar.hold
:yjbar.hold
:X1
:X2
:X3
:X4
:X5
:X6
:X7
:X8
:X9
:Qx1
:Qx2
:Qx3
:Qx4
:Qx5
:Qx6
:Qx7
:Qx8
:Qx9
:Y1
:Y2
:Y3
:Y4
:Y5
:Y6
:Y7
:Y8
:Y9
:Qy1
:Qy2
:Qy3
:Qy4
:Qy5
:Qy6
:Qy7
:Qy8
:Qy9

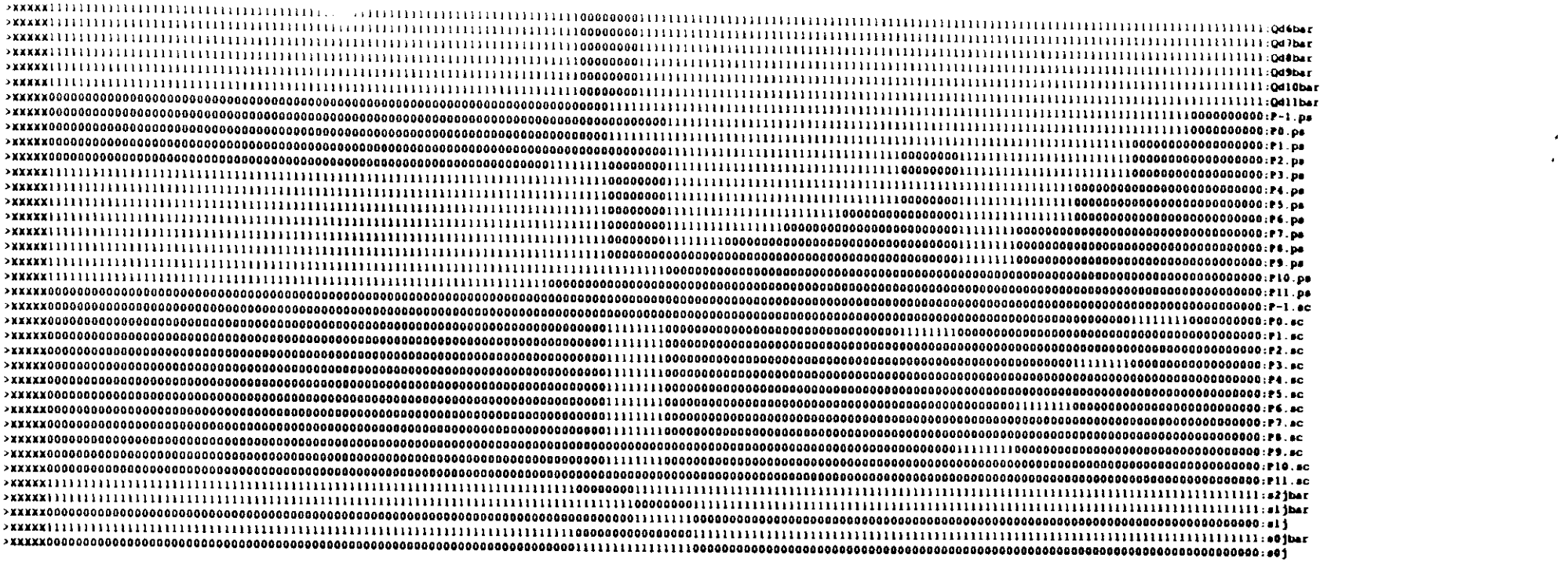

1098 transistors, 706 nodes (22 pulled up)
:phi1
:phi1bar
:phi2
:phi2bar
:ENABLE
:ENABLEbar
:GRESET
:atemp3
:atemp2
:atemp1
:atemp0
:as3
:as2
:as1
:as0
:ac3
:ac2
:ac1
:ac0
:xdbar
:passGbar
:passHbar
:shiftG
:shiftGbar
:shiftH
:shiftHbar
:mj
:yj
:mjbar.hold
:yjbar.hold

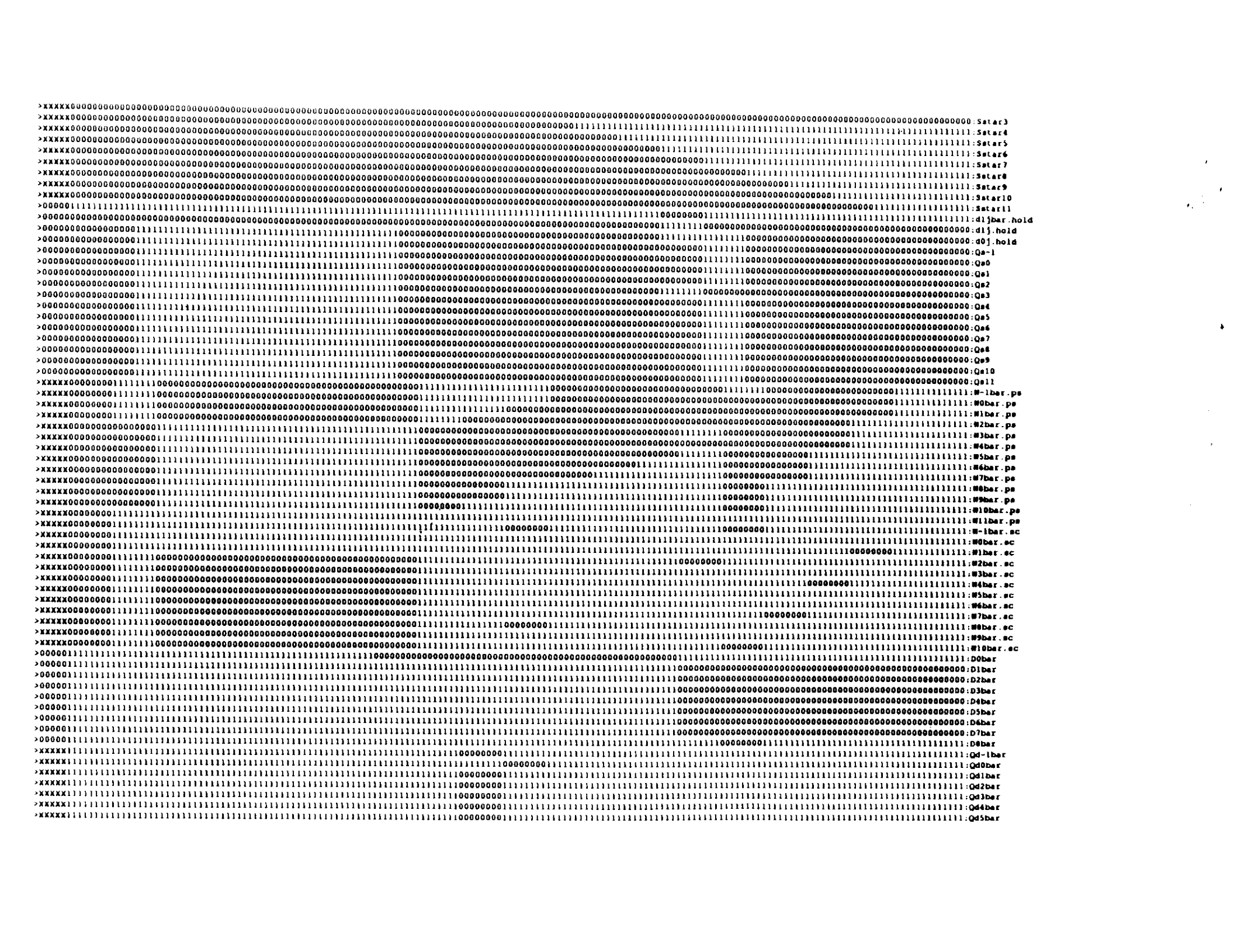

2865 transistors, 1603 nodes (17 pulled up)
phi1
phi1bar
phi2
phi2bar
GRESETbar
m-5
s-5
m-4
s-4
m-3
s-3
m-2
s-2
m-1
s-1
m0
s0
m1
s1
m2
s2
m3
s3
m4
s4
m5
s5
m6
s6
m7
s7
m8
s8
m9
s2jbar
s1jbar
s0jbar
I-2
I-1
I0
I1
I2
I3
I4
I5
I6
I7
D0bar
D1bar
D2bar
D3bar
D4bar
D5bar
D6bar
D7bar
D8bar
D0
D1
D2
D3
D4
D5
D6
D7
D8

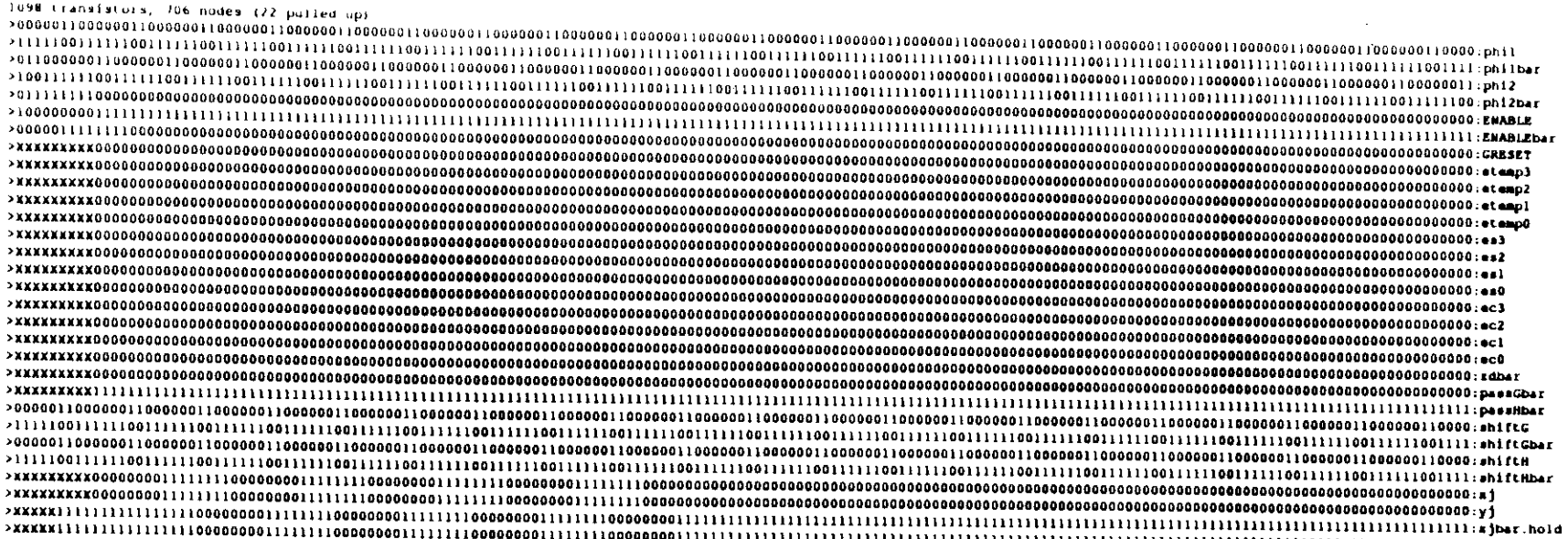



3482 transistors, 1990 nodes (14 pulled up)
phi1
phi1bar
phi2
phi2bar
ENABLE
ENABLEbar
GRESET
GRESETbar
m-6
s-6
m-5
s-5
m-4
s-4
m-3
s-3
m-2
s-2
m-1
s-1
m0
s0
m1
s1
m2
s2
m3
s3
m4
s4
m5
s5
m6
s6
m7
s7
m8
s8
m9
s9
m10
s10
m11
s11
out1
out2
out3
out4
out5
out6
out7
out8
$1
$2
$3
$4
$5
$6
$7
$8
$9
$10
$11
$star1
$star2


Datar0
Datar1
Datar2
Datar3
Datar4
Datar5
Datar6
Datar7
Datar8
Qd-1
Qd0
Qd1
Qd2
Qd3
Qd4
Qd5
Qd6
Qd7
Qd8
R-2.ps
R-1.ps
R0.ps
R1.ps
R2.ps
R3.ps
R4.ps
R5.ps
R6.ps
R7.ps
R-2.sc
R-1.sc
R0.sc
R1.sc
R2.sc
R3.sc
R4.sc
R5.sc
R6.sc
R7.sc
dljbar.latch
dlj.latch
d0j.latch
d2jbar.hold
dljbar.hold
dlj.hold
d0jbar.hold
d0j.hold


Qd6bar
Qd7bar
Qd8bar
Qd9bar
Qd10bar
Qd11bar
P-1.ps
P0.ps
P1.ps
P2.ps
P3.ps
P4.ps
P5.ps
P6.ps
P7.ps
P8.ps
P9.ps
P10.ps
P11.ps
P-1.sc
P0.sc
P1.sc
P2.sc
P3.sc
P4.sc
P5.sc
P6.sc
P7.sc
P8.sc
P9.sc
P10.sc
P11.sc
s2jbar
s1jbar
s1j
s0jbar
s0j




1098 transistors, 706 nodes (72 pulled up)
:phi1
:phi1bar
:phi2
:phi2bar
:ENABLE
:ENABLEbar
:GRESET
:atemp3
:atemp2
:atemp1
:atemp0
:as3
:as2
:as1
:as0
:ac3
:ac2
:ac1
:ac0
:adbar
:passGbar
:passHbar
:shiftG
:shiftGbar
:shiftH
:shiftHbar
:aj
:yj
:ajbar.hold
:yjbar.hold

maui:faris

case5.out

Sat Dec 3 22:42:44 1988

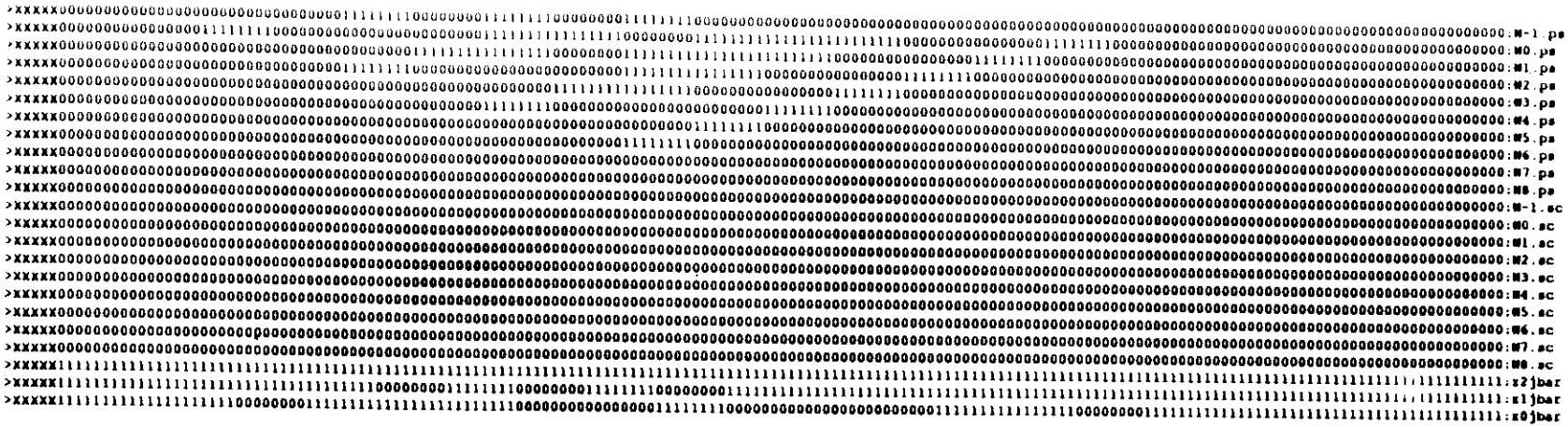
pub3 / Public 3

pub3 maui:faris Job: case5.out Date: Sat Dec 3 22:42:44 1988

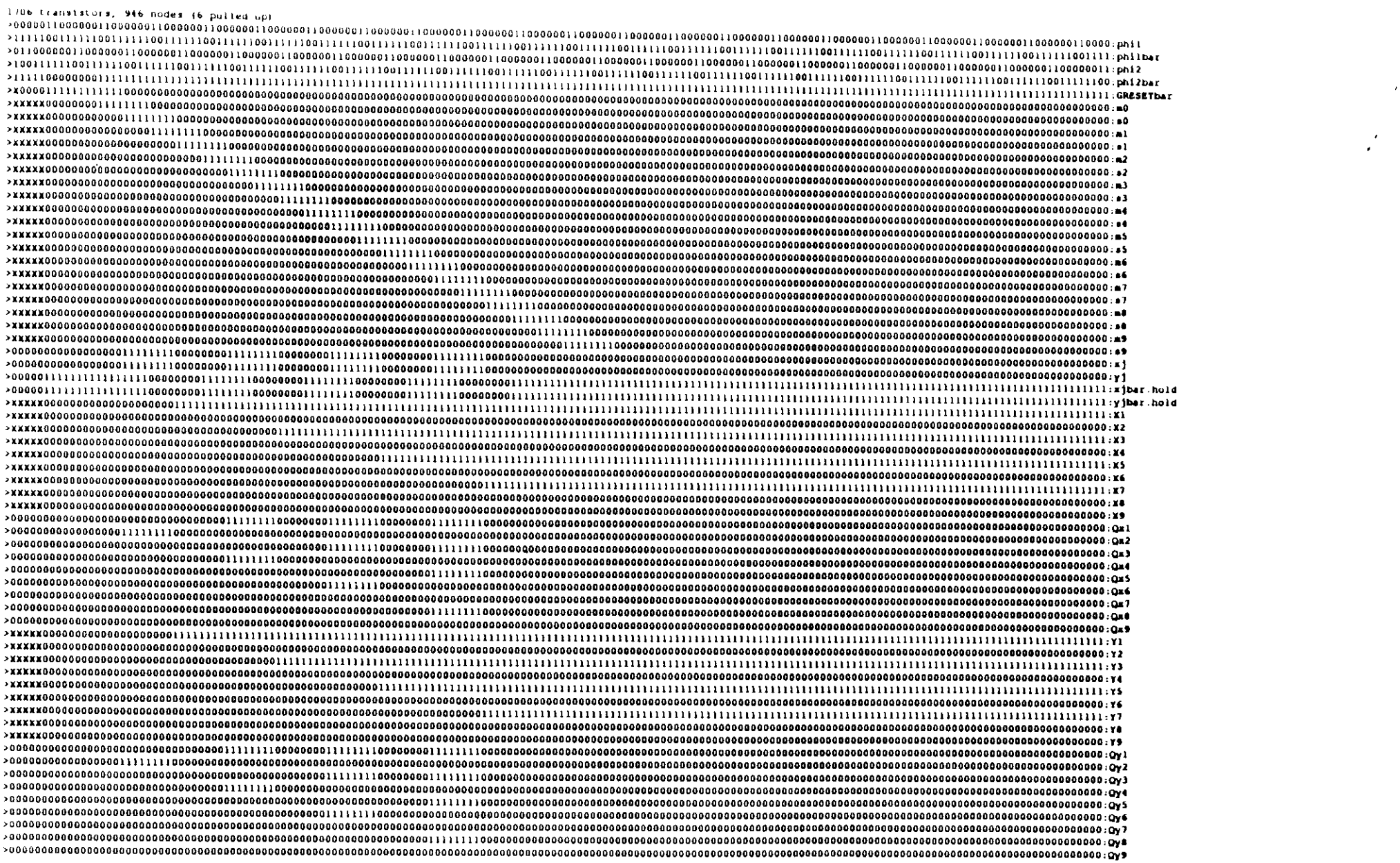
pub3 maui:faris Job: case5.out Date: Sat Dec 3 22:42:44 1988

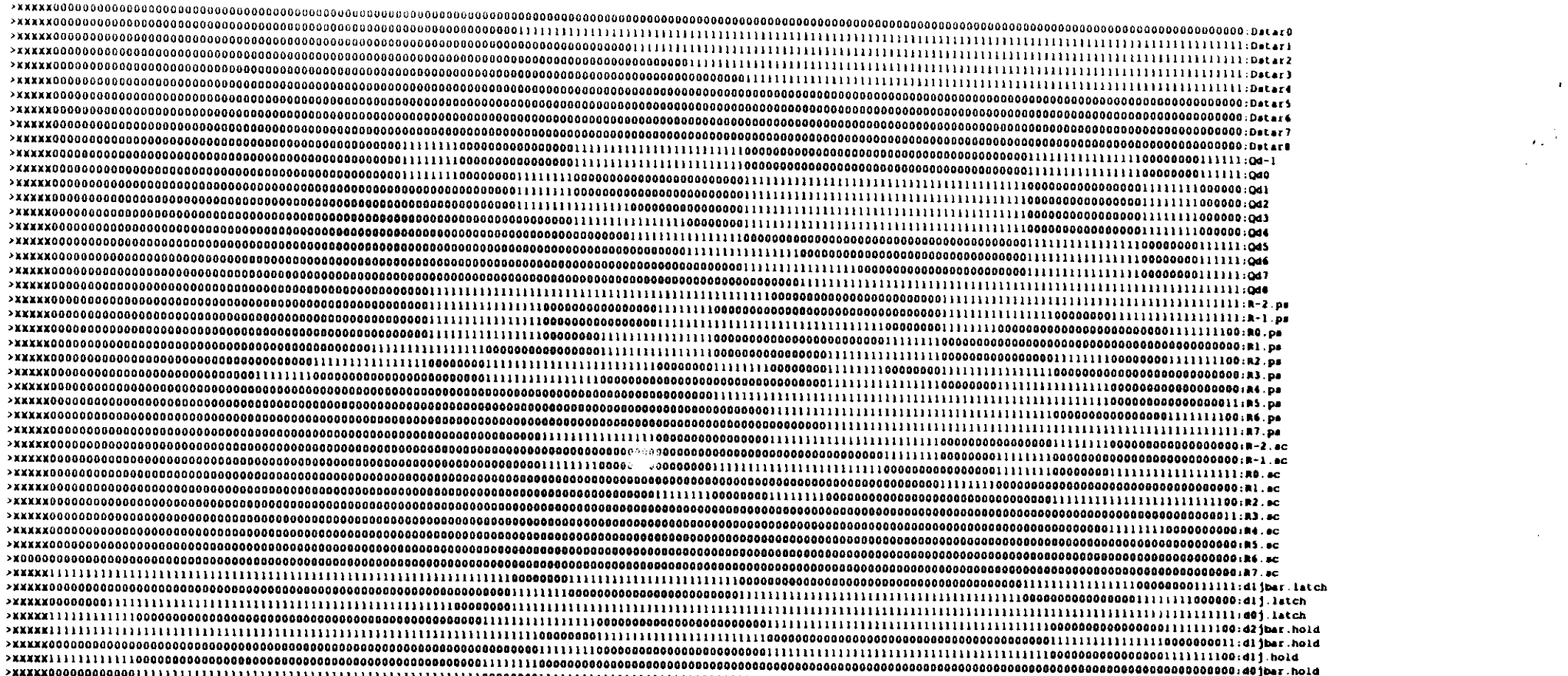
pub3 maui:faris Job: case5.out Date: Sat Dec 3 22:42:44 1988

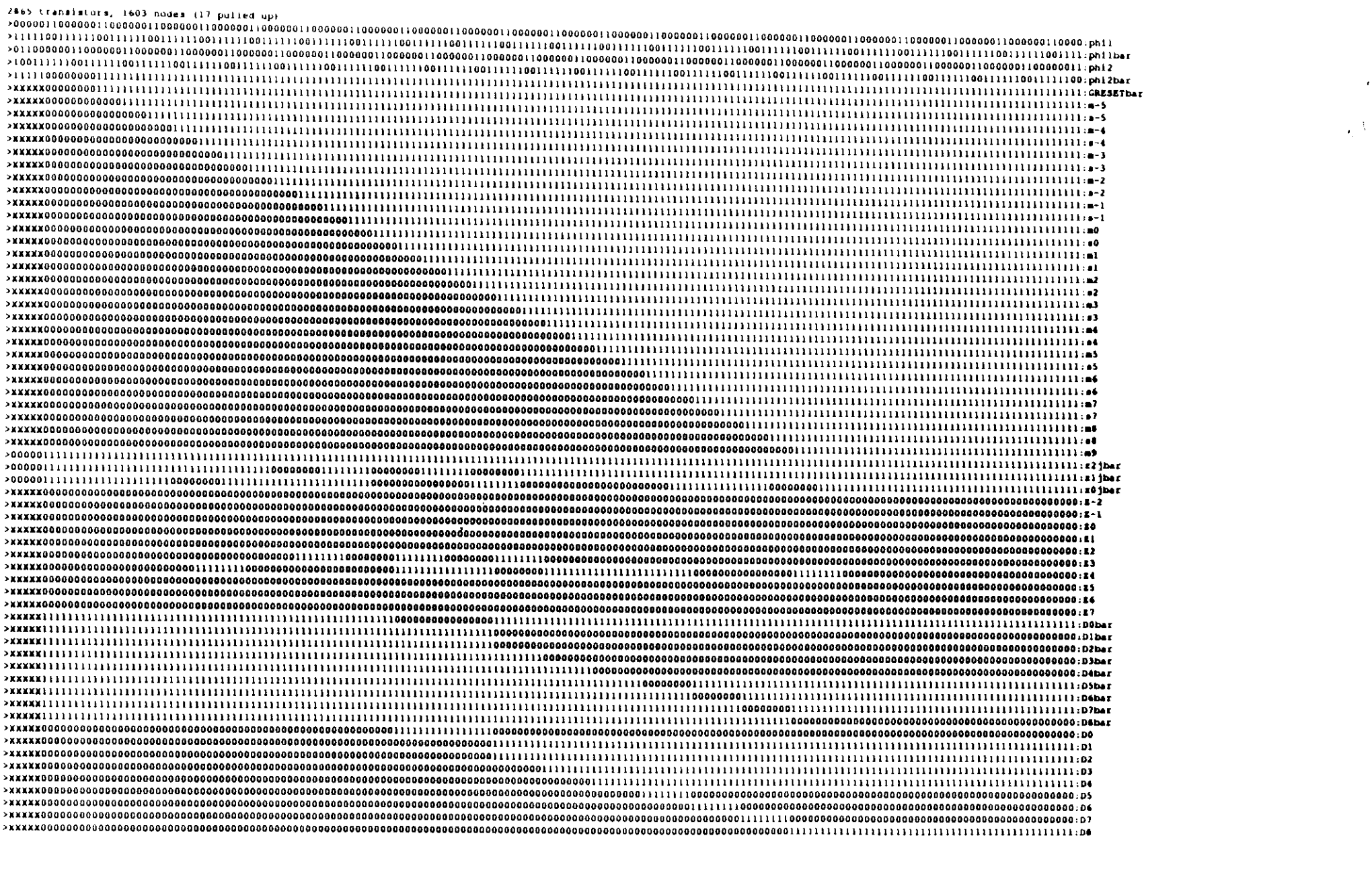
pub3 maui:faris Job: case5.out Date: Sat Dec 3 22:42:44 1988

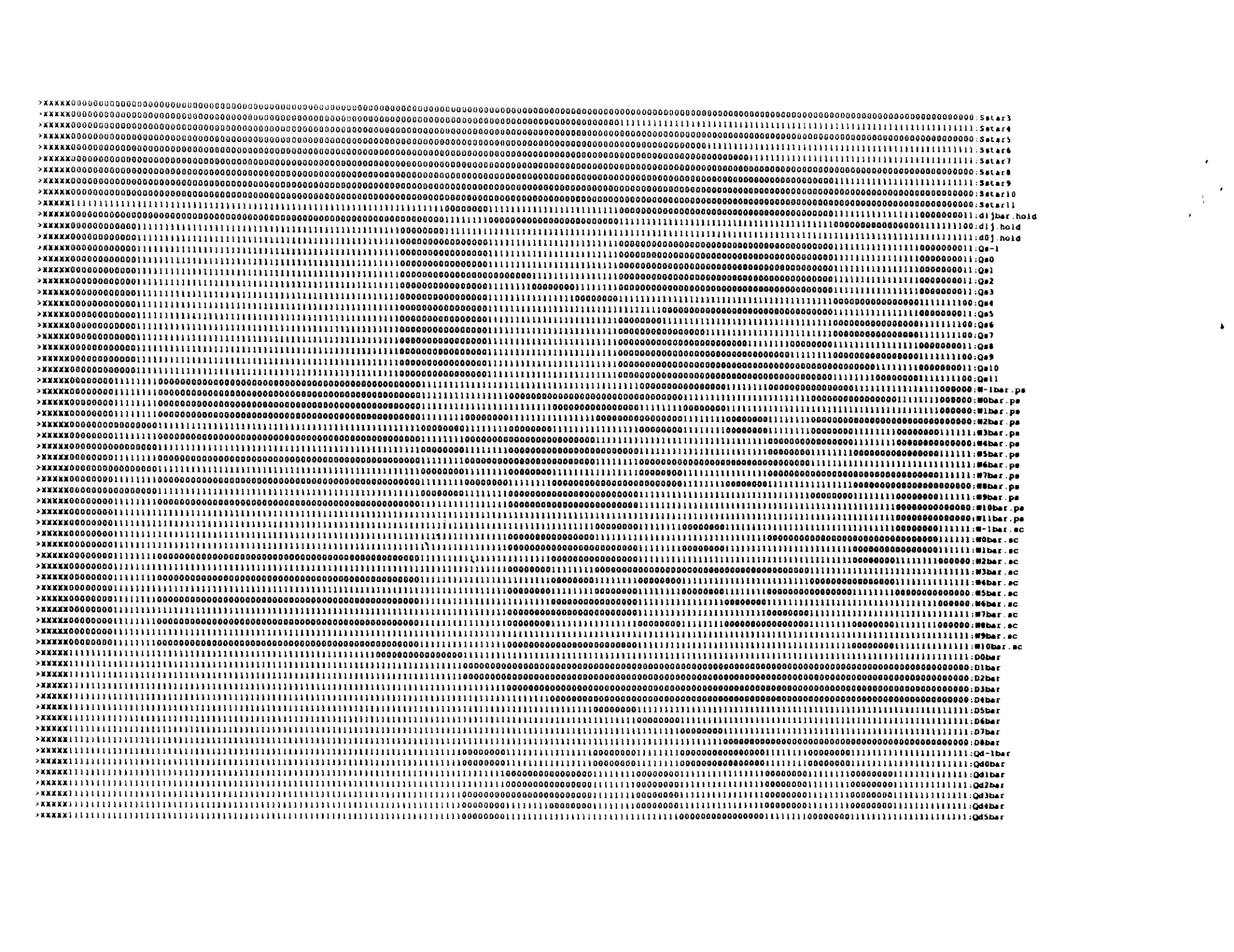

M-1.ps
M0.ps
M1.ps
M2.ps
M3.ps
M4.ps
M5.ps
M6.ps
M7.ps
M8.ps
M-1.sc
M0.sc
M1.sc
M2.sc
M3.sc
M4.sc
M5.sc
M6.sc
M7.sc
M8.sc
x2jbar
x1jbar
x0jbar

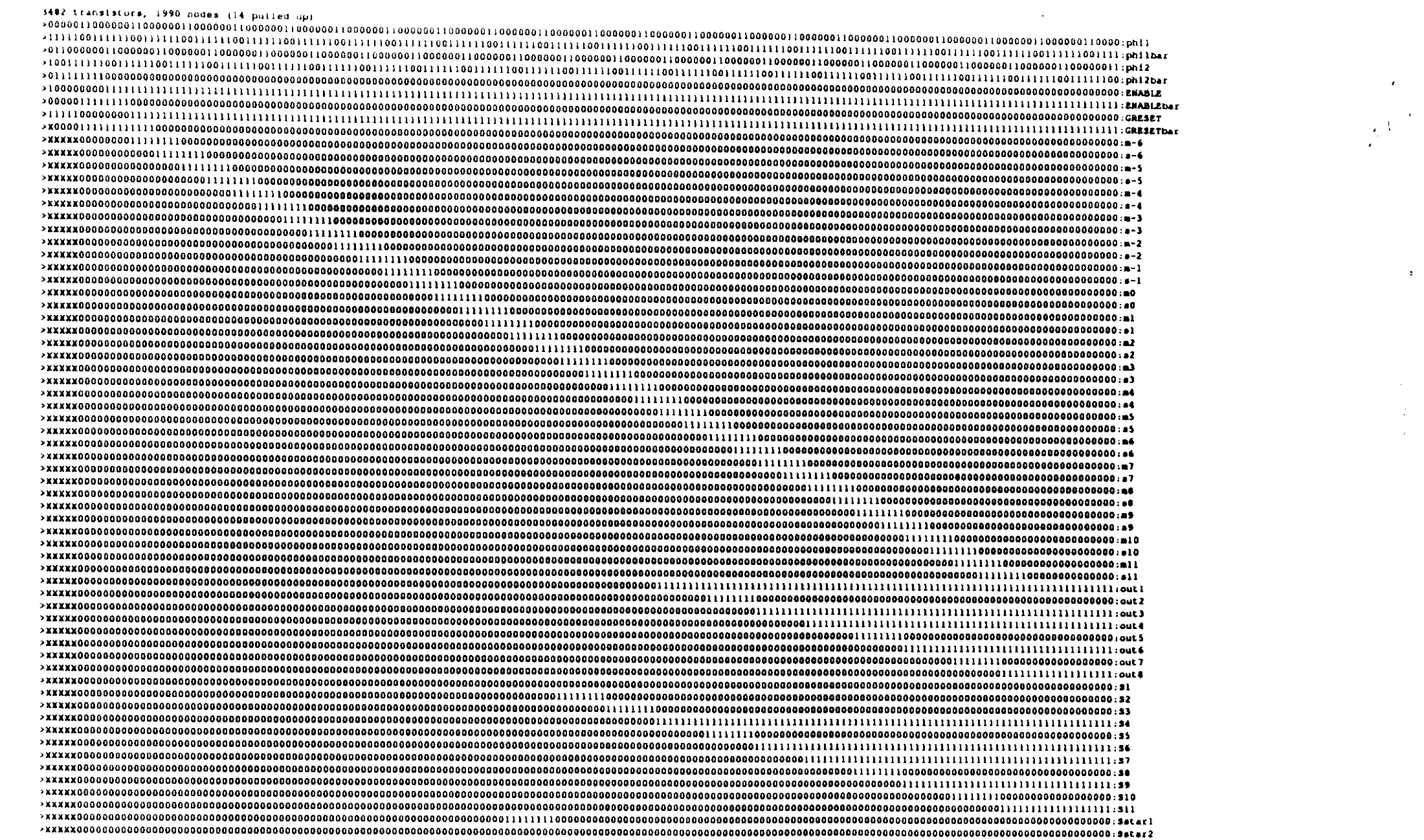
1706 transistors, 946 nodes (6 pulled up)




Dstar0
Dstar1
Dstar2
Dstar3
Dstar4
Dstar5
Dstar6
Dstar7
Dstar8
Qd-1
Qd0
Qd1
Qd2
Qd3
Qd4
Qd5
Qd6
Qd7
Qd8
R-2.ps
R-1.ps
R0.ps
R1.ps
R2.ps
R3.ps
R4.ps
R5.ps
R6.ps
R7.ps
R-2.sc
R-1.sc
R0.sc
R1.sc
R2.sc
R3.sc
R4.sc
R5.sc
R6.sc
R7.sc
dljbar.latch
dlj.latch
d0j.latch
d2jbar.hold
dljbar.hold
dlj.hold
d0jbar.hold
d0j.hold


2865 transistors, 1603 nodes (17 pulled up)
:phi1
:phi1bar
:phi2
:phi2bar
:GRESETbar
:m-5
:s-5
:m-4
:s-4
:m-3
:s-3
:m-2
:s-2
:m-1
:s-1
:m0
:s0
:m1
:s1
:m2
:s2
:m3
:s3
:m4
:s4
:m5
:s5
:m6
:s6
:m7
:s7
:m8
:s8
:m9
:s2jbar
:s1jbar
:s0jbar
:E-2
:E-1
:E0
:E1
:E2
:E3
:E4
:E5
:E6
:E7
:D0bar
:D1bar
:D2bar
:D3bar
:D4bar
:D5bar
:D6bar
:D7bar
:D8bar
:D0
:D1
:D2
:D3
:D4
:D5
:D6
:D7
:D8




5482 transistors, 1990 nodes (14 pulled up)
:phi1
:phi1bar
:phi2
:phi2bar
:ENABLE
:ENABLEbar
:GRESET
:GRESETbar
:m-6
:s-6
:m-5
:s-5
:m-4
:s-4
:m-3
:s-3
:m-2
:s-2
:m-1
:s-1
:m0
:s0
:m1
:s1
:m2
:s2
:m3
:s3
:m4
:s4
:m5
:s5
:m6
:s6
:m7
:s7
:m8
:s8
:m9
:s9
:m10
:s10
:m11
:s11
:out1
:out2
:out3
:out4
:out5
:out6
:out7
:out8
:$1
:$2
:$3
:$4
:$5
:$6
:$7
:$8
:$9
:$10
:$11
:$star1
:$star2

maui:faris

case6.out

Sat Dec 3 22:43:31 1988

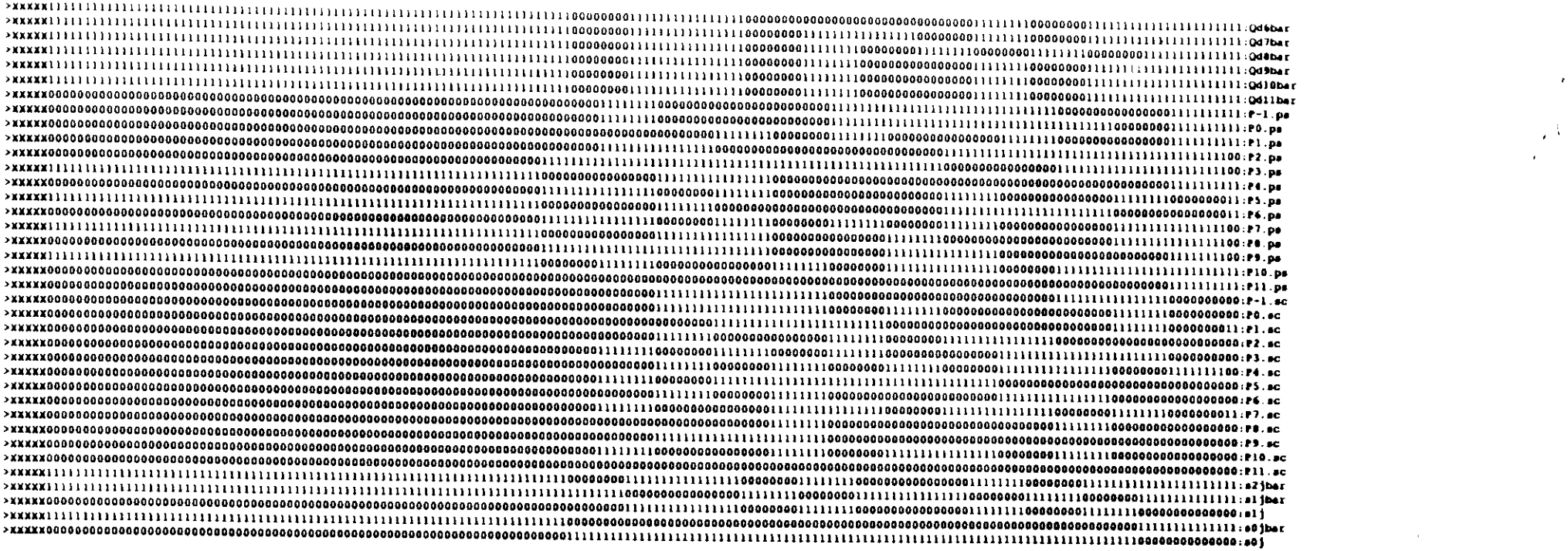
pub3 / Public 3

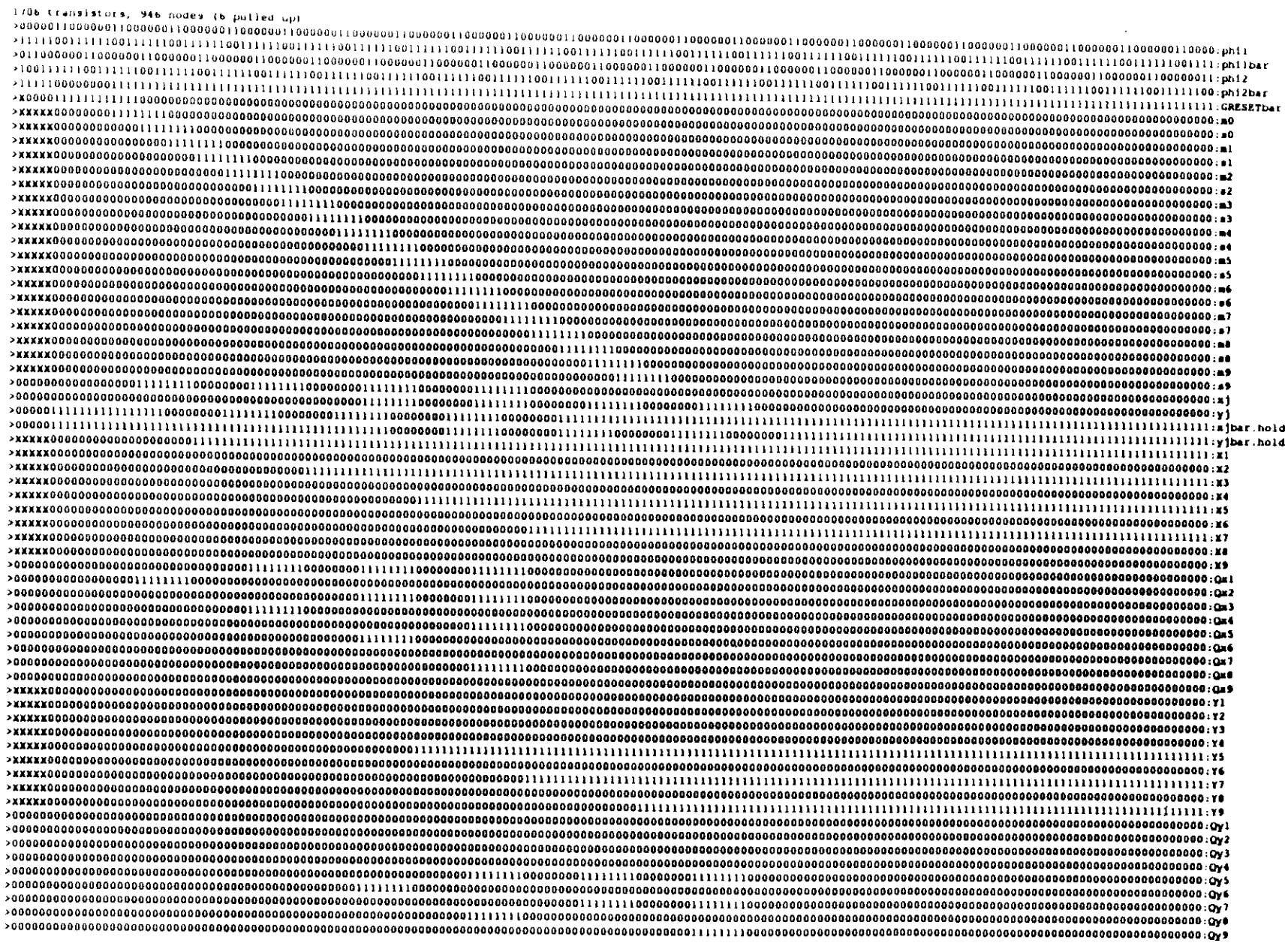
pub3 maui:faris Job: case6.out Date: Sat Dec 3 22:43:31 1988

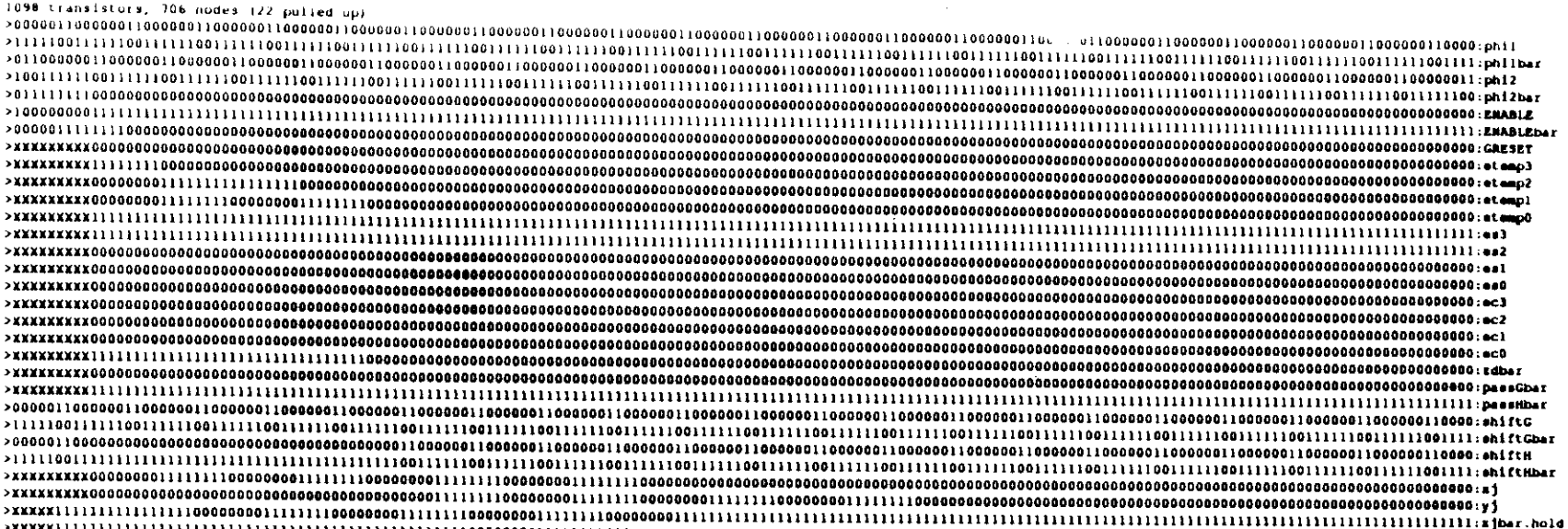
pub3 maui:faris Job: case6.out Date: Sat Dec 3 22:43:31 1988

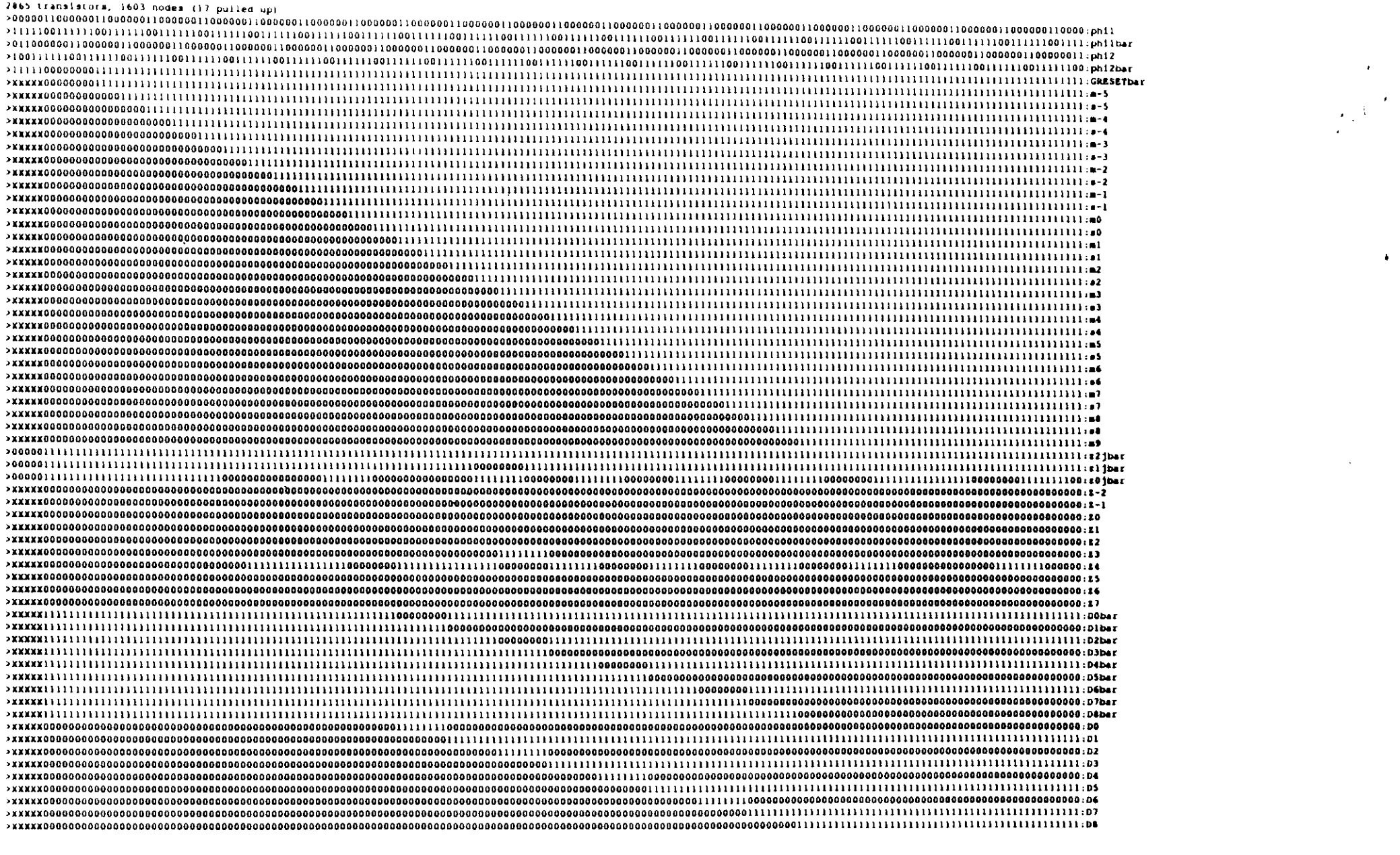
pub3 maui:faris Job: case6.out Date: Sat Dec 3 22:43:31 1988

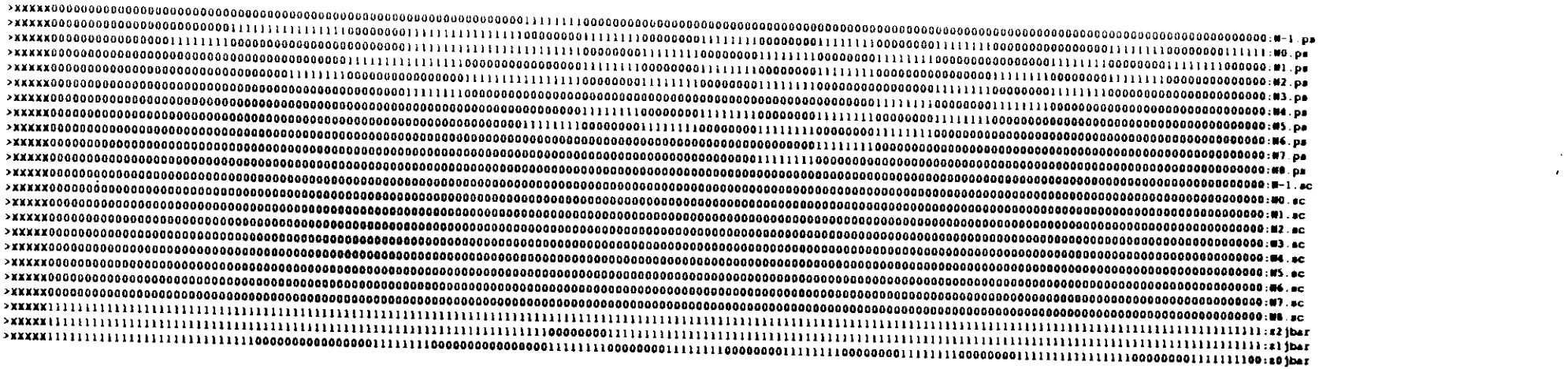
pub3 maui:faris Job: case6.out Date: Sat Dec 3 22:43:31 1988

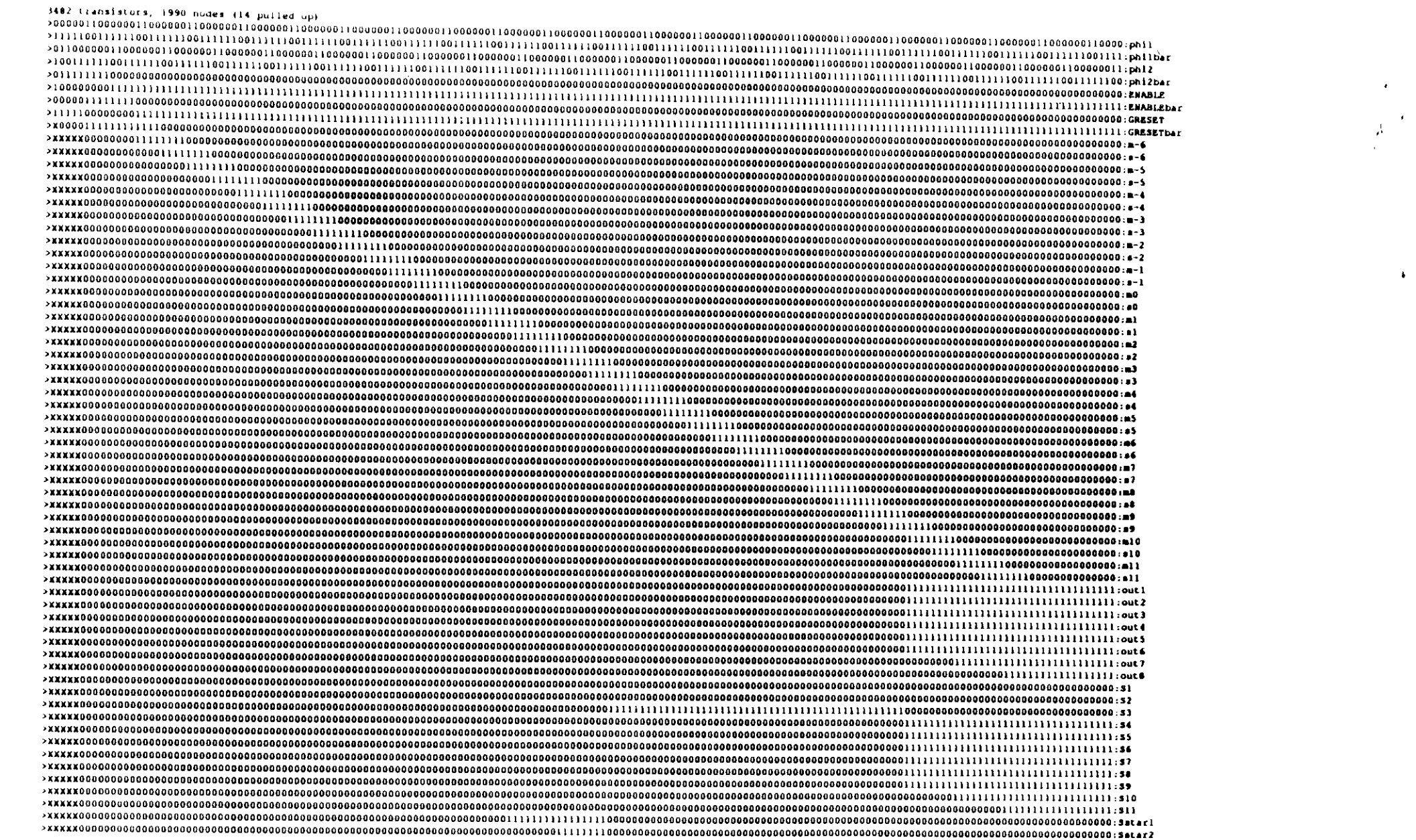

Qd6bar
Qd7bar
Qd8bar
Qd9bar
Qd10bar
Qd11bar
P-1.ps
P0.ps
P1.ps
P2.ps
P3.ps
P4.ps
P5.ps
P6.ps
P7.ps
P8.ps
P9.ps
P10.ps
P11.ps
P-1.sc
P0.sc
P1.sc
P2.sc
P3.sc
P4.sc
P5.sc
P6.sc
P7.sc
P8.sc
P9.sc
P10.sc
P11.sc
s2jbar
s1jbar
s1j
s0jbar
s0j

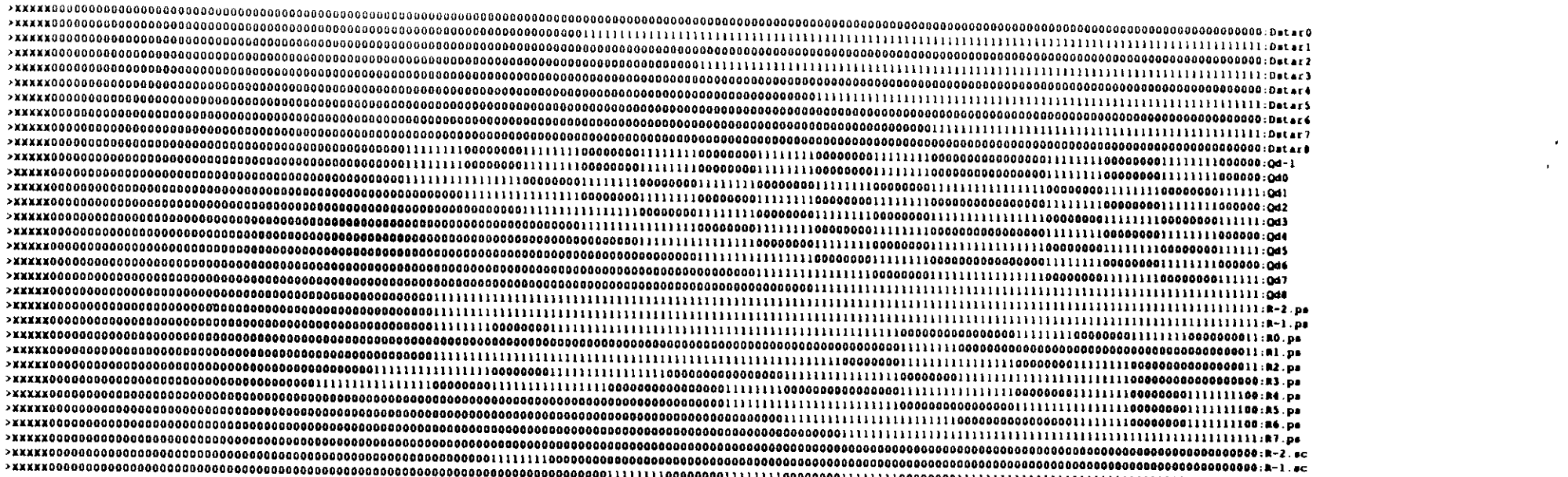

1706 transistors, 946 nodes (6 pulled up)
:phi1
:phi1bar
:phi2
:phi2bar
:GRESETbar
:m0
:s0
:m1
:s1
:m2
:s2
:m3
:s3
:m4
:s4
:m5
:s5
:m6
:s6
:m7
:s7
:m8
:s8
:m9
:s9
:xj
:yj
:xjbar.hold
:yjbar.hold
:X1
:X2
:X3
:X4
:X5
:X6
:X7
:X8
:X9
:Qx1
:Qx2
:Qx3
:Qx4
:Qx5
:Qx6
:Qx7
:Qx8
:Qx9
:Y1
:Y2
:Y3
:Y4
:Y5
:Y6
:Y7
:Y8
:Y9
:Qy1
:Qy2
:Qy3
:Qy4
:Qy5
:Qy6
:Qy7
:Qy8
:Qy9

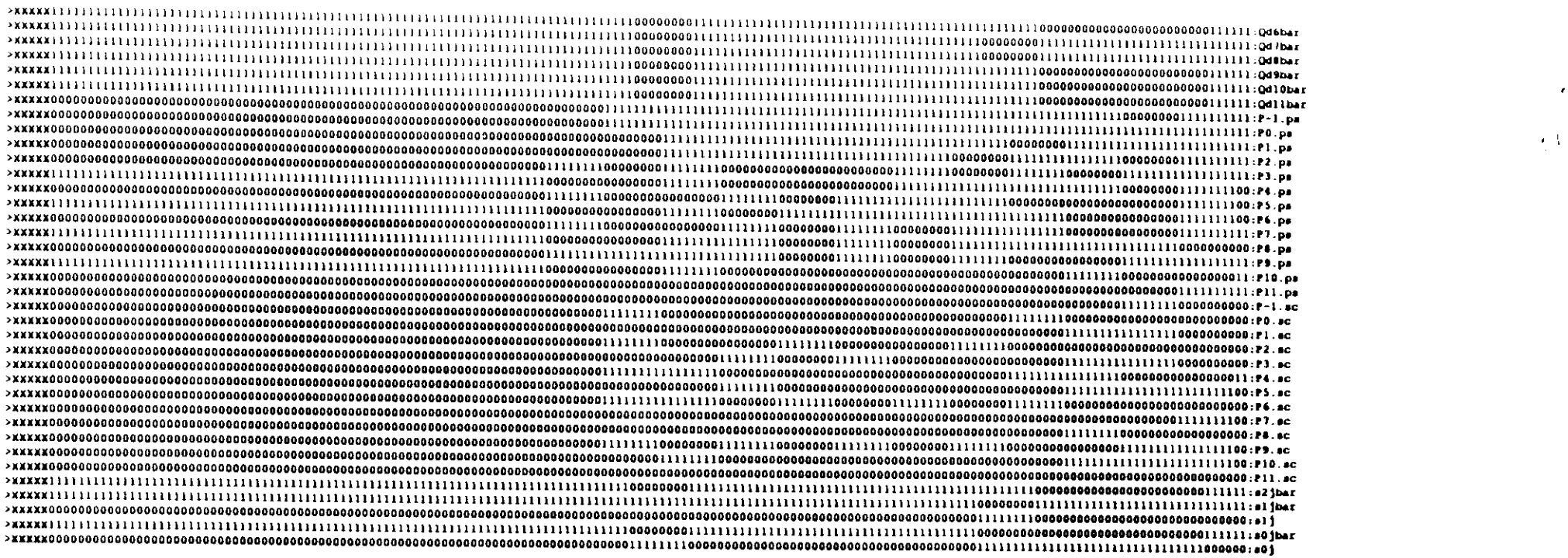

1098 transistors, 706 nodes (22 pulled up)
:phi1
:phi1bar
:phi2
:phi2bar
:ENABLE
:ENABLEbar
:GRESET
:atemp3
:atemp2
:atemp1
:atemp0
:as3
:as2
:as1
:as0
:ac3
:ac2
:ac1
:ac0
:tdbar
:passGbar
:passHbar
:shiftG
:shiftGbar
:shiftH
:shiftHbar
:xj
:yj
:xjbar.hold
:yjbar.hold

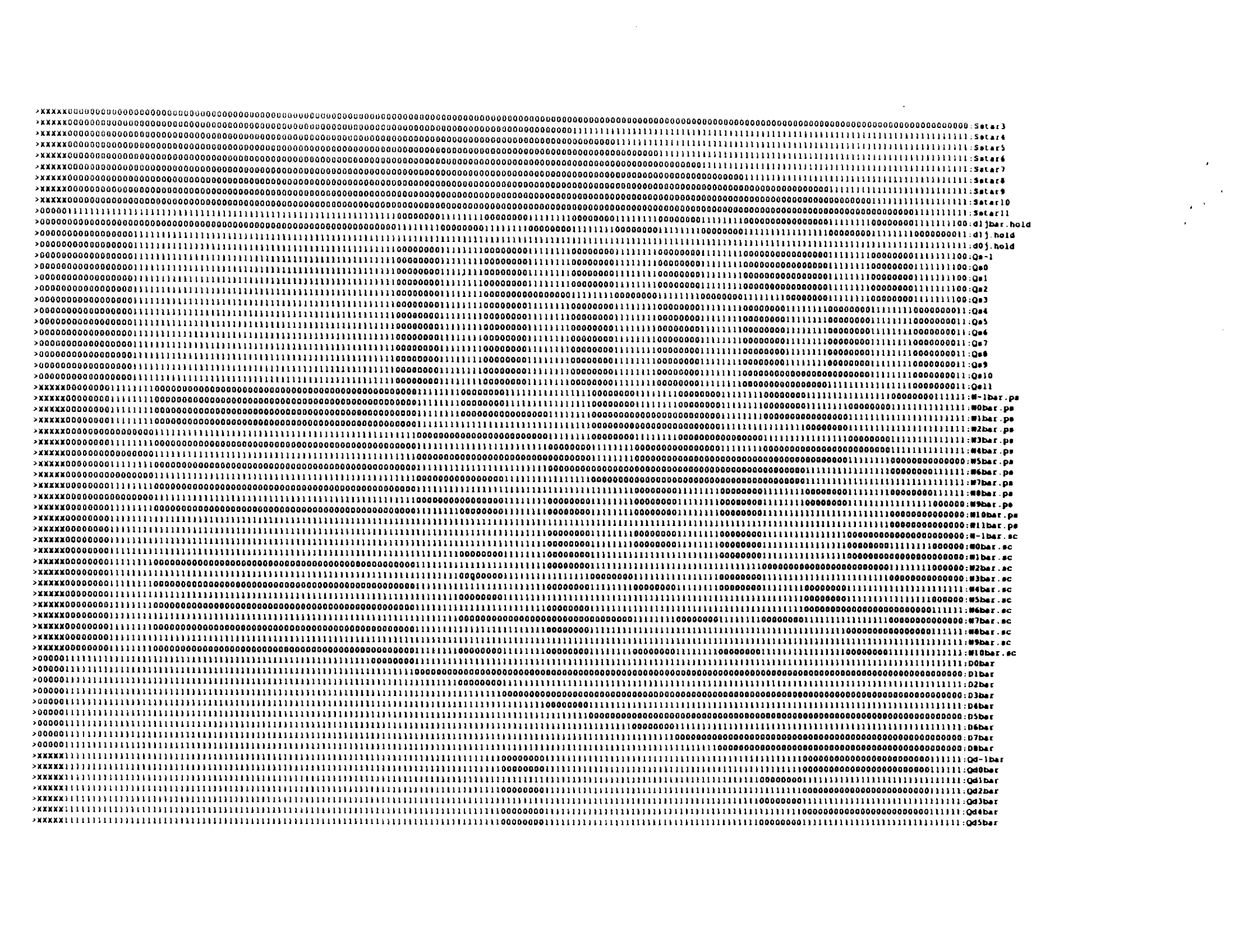

2865 transistors, 1603 nodes (17 pulled up)
phi1
phi1bar
phi2
phi2bar
GRESETbar
m-5
s-5
m-4
s-4
m-3
s-3
m-2
s-2
m-1
s-1
m0
s0
m1
s1
m2
s2
m3
s3
m4
s4
m5
s5
m6
s6
m7
s7
m8
s8
m9
s2jbar
s1jbar
s0jbar
Z-2
Z-1
Z0
Z1
Z2
Z3
Z4
Z5
Z6
Z7
D0bar
D1bar
D2bar
D3bar
D4bar
D5bar
D6bar
D7bar
D8bar
D0
D1
D2
D3
D4
D5
D6
D7
D8

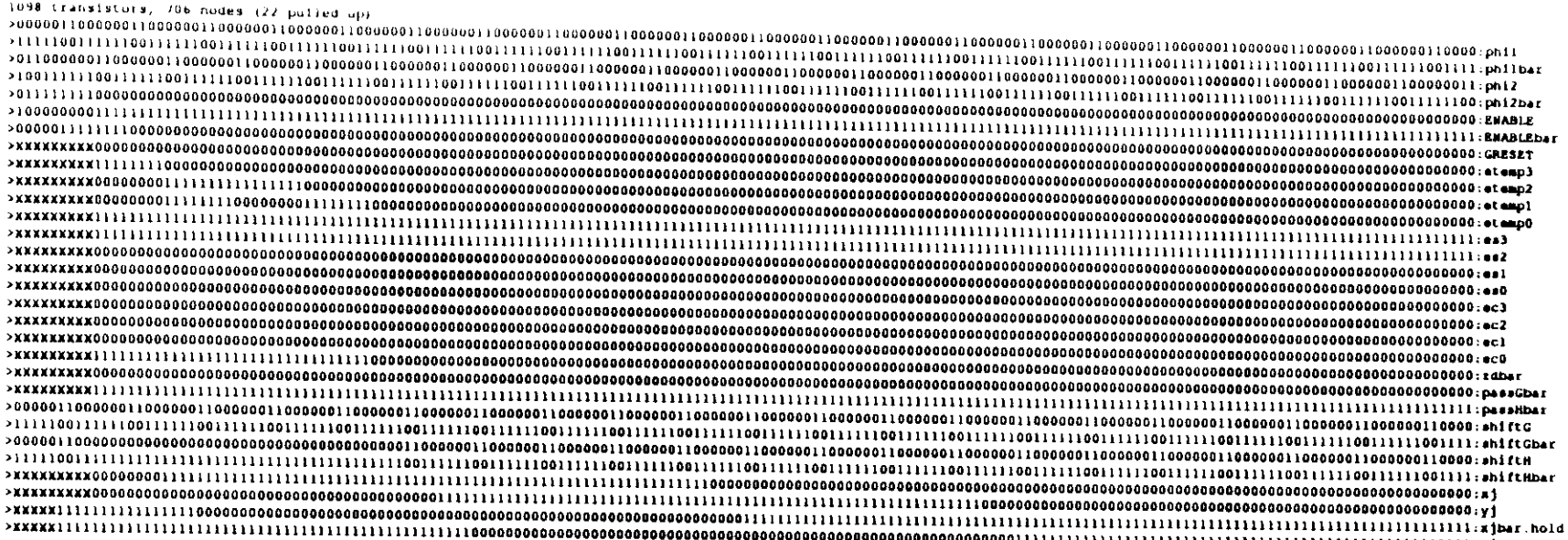

M-1.ps
M0.ps
M1.ps
M2.ps
M3.ps
M4.ps
M5.ps
M6.ps
M7.ps
M8.ps
M-1.sc
M0.sc
M1.sc
M2.sc
M3.sc
M4.sc
M5.sc
M6.sc
M7.sc
M8.sc
z2jbar
z1jbar
z0jbar


3402 transistors, 1990 nodes (14 pulled up)
:phi1
:phi1bar
:phi2
:phi2bar
:ENABLE
:ENABLEbar
:GRESET
:GRESETbar
:m-6
:s-6
:m-5
:s-5
:m-4
:s-4
:m-3
:s-3
:m-2
:s-2
:m-1
:s-1
:m0
:s0
:m1
:s1
:m2
:s2
:m3
:s3
:m4
:s4
:m5
:s5
:m6
:s6
:m7
:s7
:m8
:s8
:m9
:s9
:m10
:s10
:m11
:s11
:out1
:out2
:out3
:out4
:out5
:out6
:out7
:out8
:S1
:S2
:S3
:S4
:S5
:S6
:S7
:S8
:S9
:S10
:S11
:Satar1
:Satar2


Dstar0
Dstar1
Dstar2
Dstar3
Dstar4
Dstar5
Dstar6
Dstar7
Dstar8
Qd-1
Qd0
Qd1
Qd2
Qd3
Qd4
Qd5
Qd6
Qd7
Qd8
R-2.ps
R-1.ps
R0.ps
R1.ps
R2.ps
R3.ps
R4.ps
R5.ps
R6.ps
R7.ps
R-2.sc
R-1.sc
R0.sc
R1.sc
R2.sc
R3.sc
R4.sc
R5.sc
R6.sc
R7.sc
d1jbar.latch
d1j.latch
d0j.latch
d2jbar.hold
d1jbar.hold
d1j.hold
d0jbar.hold
d0j.hold


Qd6bar
Qd7bar
Qd8bar
Qd9bar
Qd10bar
Qd11bar
P-1.ps
P0.ps
P1.ps
P2.ps
P3.ps
P4.ps
P5.ps
P6.ps
P7.ps
P8.ps
P9.ps
P10.ps
P11.ps
P-1.sc
P0.sc
P1.sc
P2.sc
P3.sc
P4.sc
P5.sc
P6.sc
P7.sc
P8.sc
P9.sc
P10.sc
P11.sc
s2jbar
s1jbar
s1j
s0jbar
s0j




1098 transistors, 706 nodes (22 pulled up)
phi1
phi1bar
phi2
phi2bar
ENABLE
ENABLEbar
GRESET
atemp3
atemp2
atemp1
atemp0
es3
es2
es1
es0
ec3
ec2
ec1
ec0
zdbar
passGbar
passHbar
shiftG
shiftGbar
shiftH
shiftHbar
xj
yj
xjbar.hold
yjbar.hold

maui:faris

case7.out

Sat Dec 3 22:44:05 1988

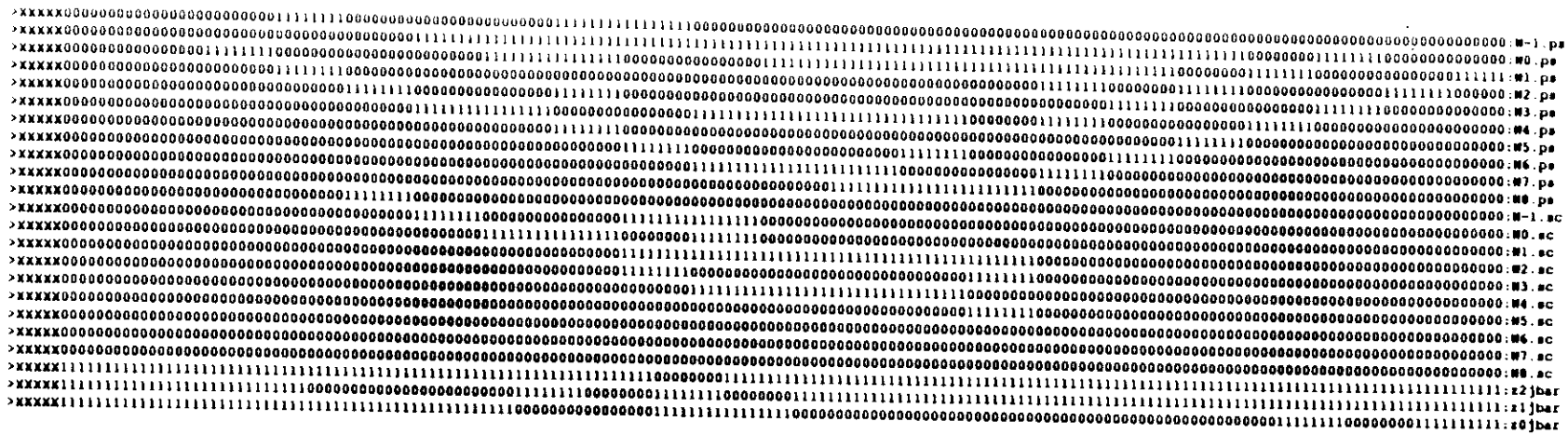
pub3 / Public 3

pub3 maui:faris Job: case7.out Date: Sat Dec 3 22:44:05 1988

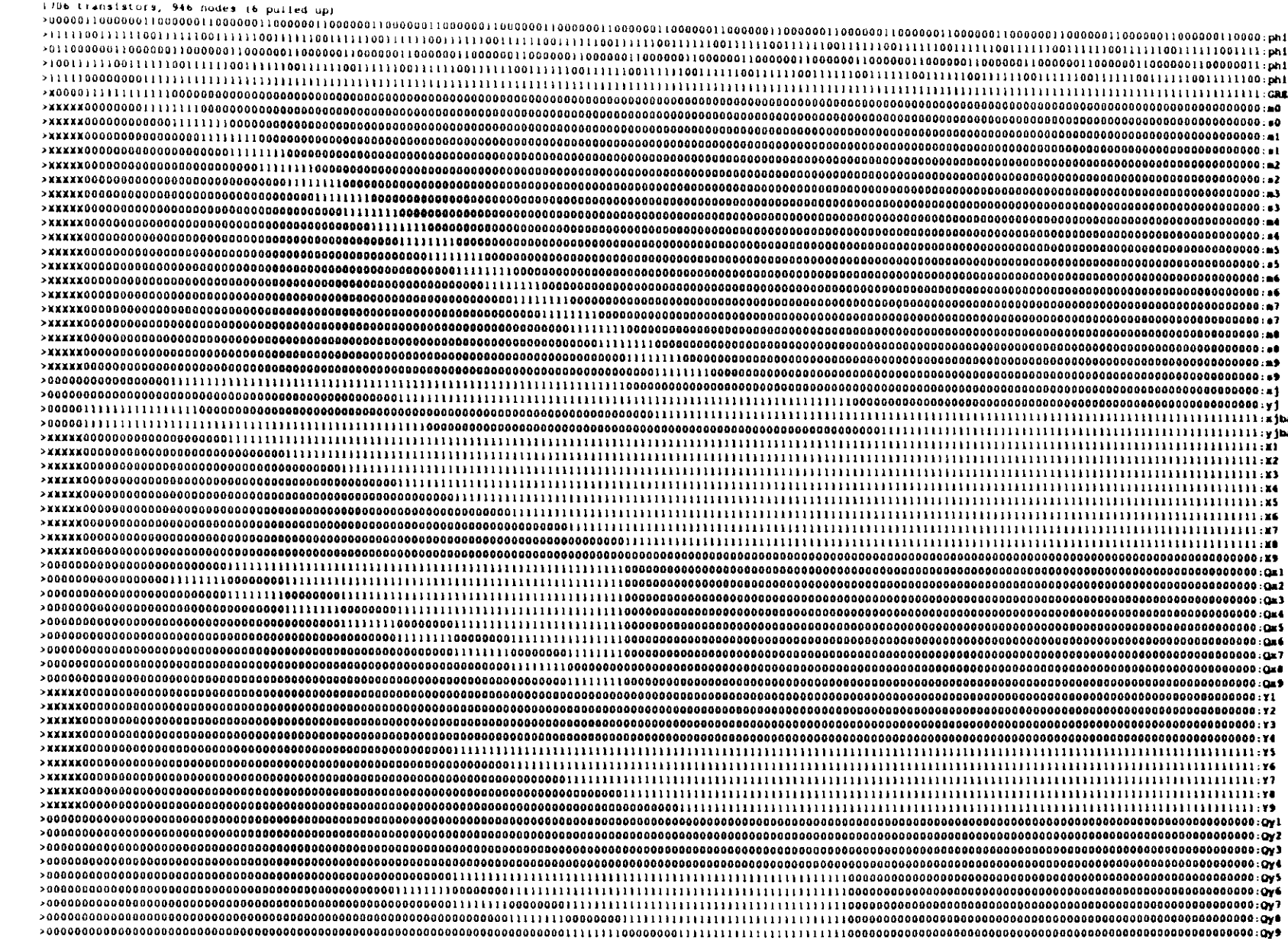
pub3 maui:faris Job: case7.out Date: Sat Dec 3 22:44:05 1988

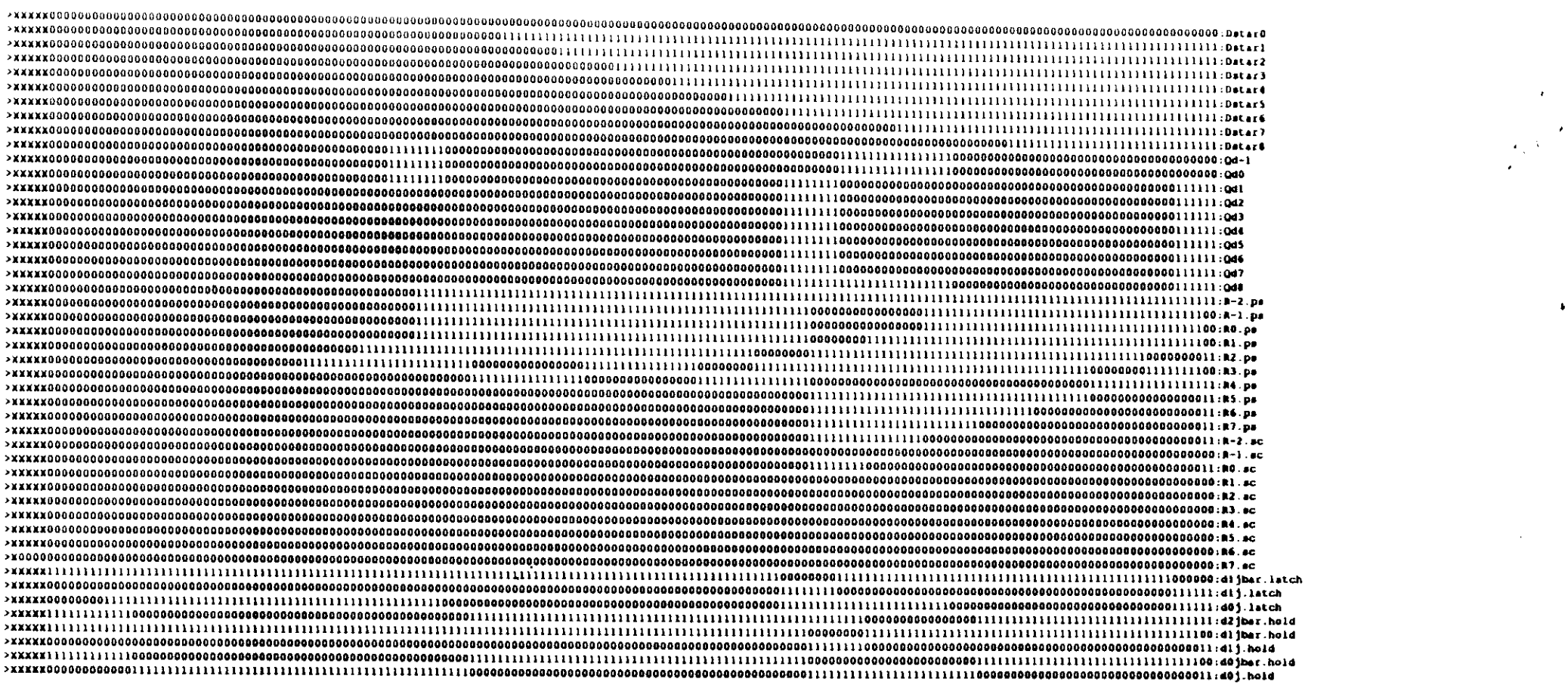
pub3 maui:faris Job: case7.out Date: Sat Dec 3 22:44:05 1988

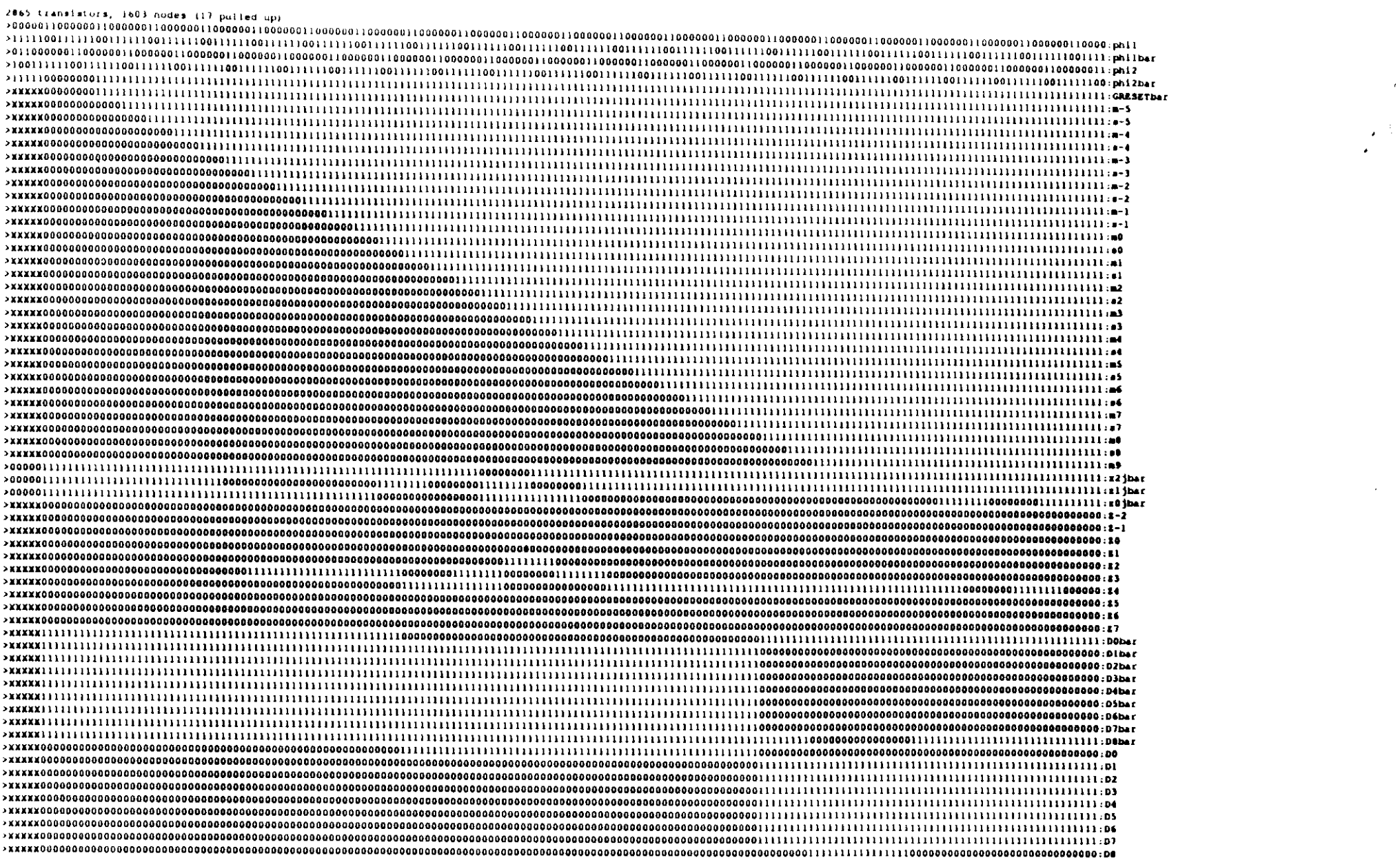
pub3 maui:faris Job: case7.out Date: Sat Dec 3 22:44:05 1988

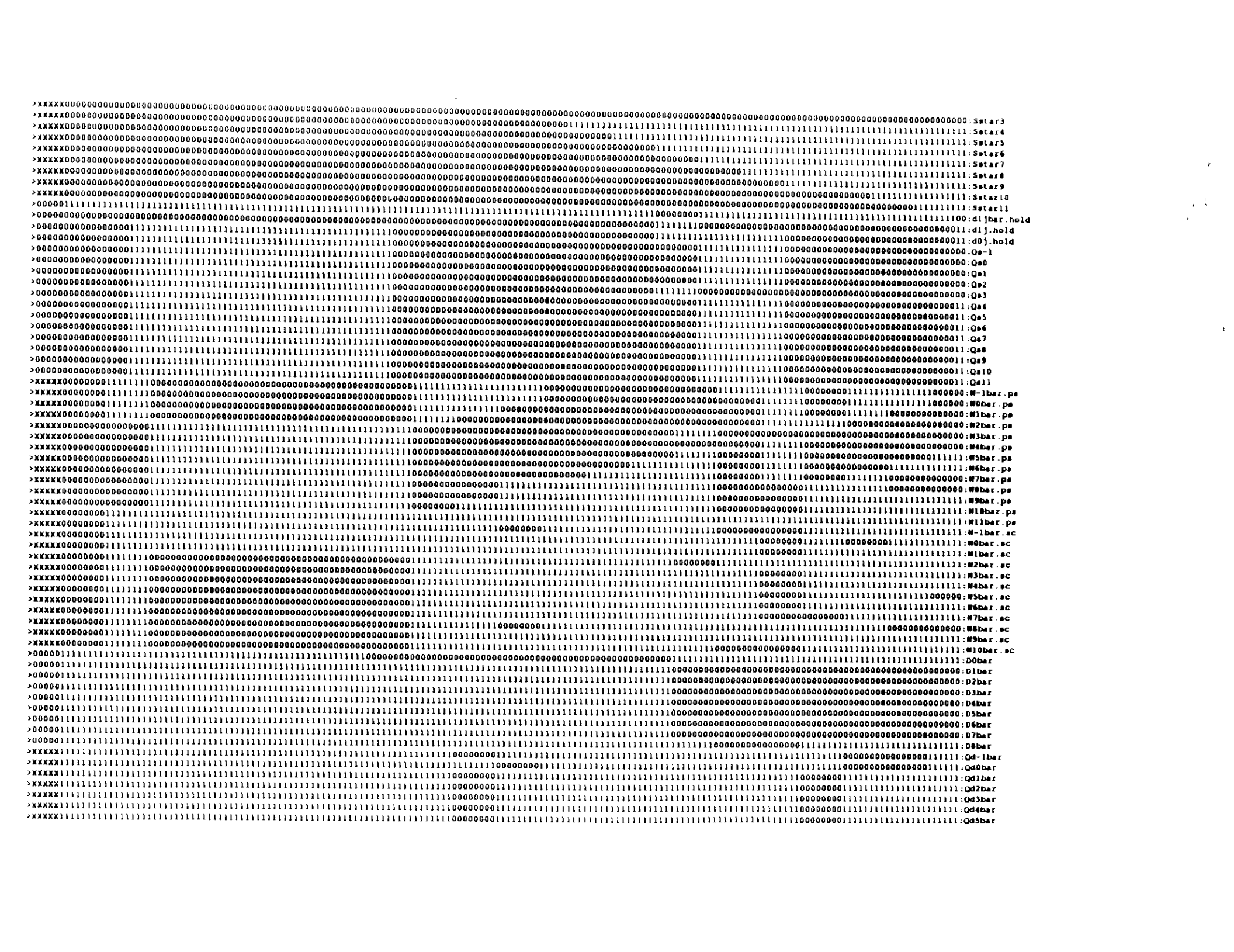

W-1.ps
W0.ps
W1.ps
W2.ps
W3.ps
W4.ps
W5.ps
W6.ps
W7.ps
W8.ps
W-1.sc
W0.sc
W1.sc
W2.sc
W3.sc
W4.sc
W5.sc
W6.sc
W7.sc
W8.sc
z2jbar
z1jbar
z0jbar

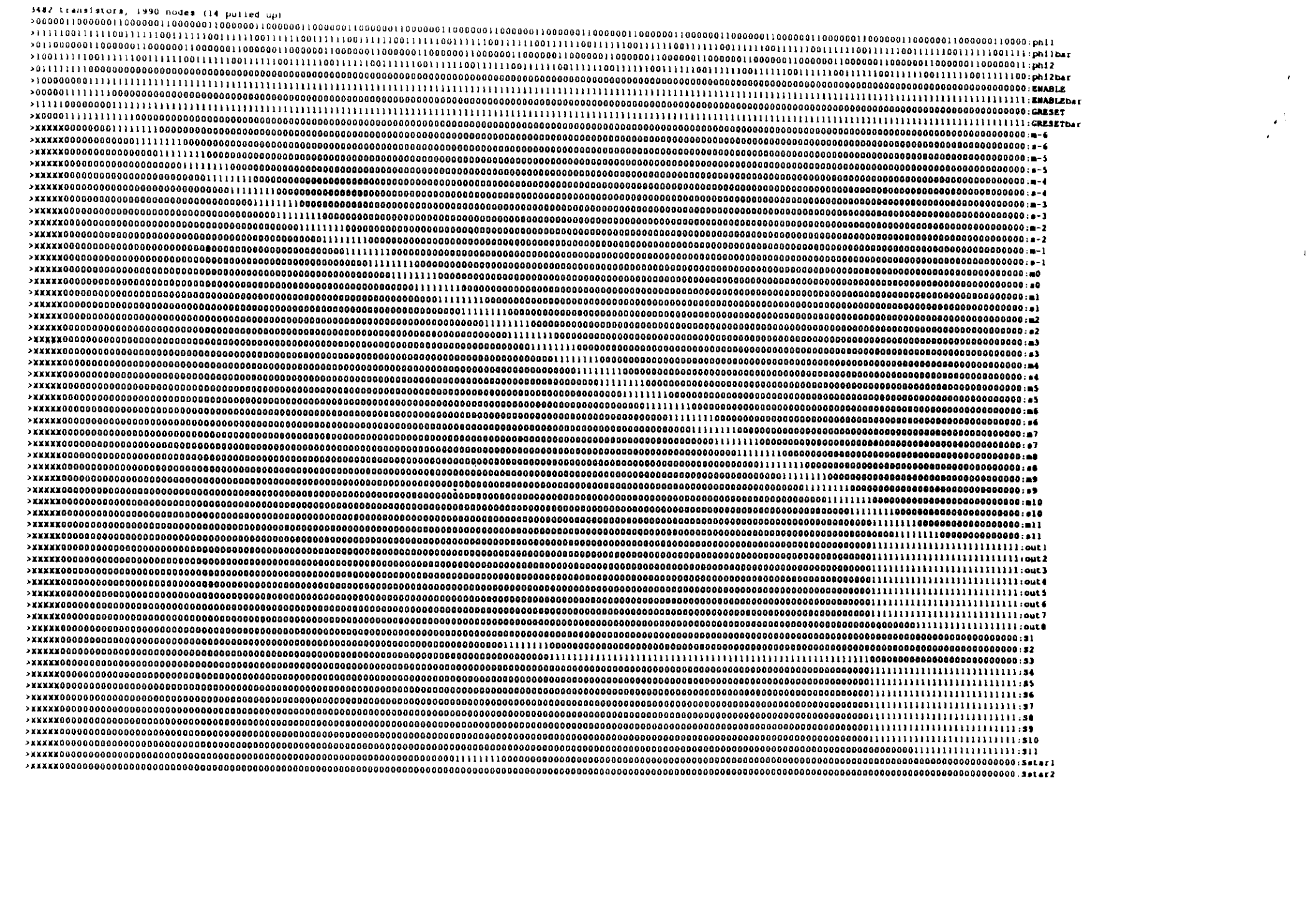
1706 transistors, 946 nodes (6 pulled up)




Dstar0
Dstar1
Dstar2
Dstar3
Dstar4
Dstar5
Dstar6
Dstar7
Dstar8
Qd-1
Qd0
Qd1
Qd2
Qd3
Qd4
Qd5
Qd6
Qd7
Qd8
R-2.ps
R-1.ps
R0.ps
R1.ps
R2.ps
R3.ps
R4.ps
R5.ps
R6.ps
R7.ps
R-2.sc
R-1.sc
R0.sc
R1.sc
R2.sc
R3.sc
R4.sc
R5.sc
R6.sc
R7.sc
d1jbar.latch
d1j.latch
d0j.latch
d2jbar.hold
d1jbar.hold
d1j.hold
d0jbar.hold
d0j.hold


2865 transistors, 1603 nodes (17 pulled up)
phi1
phi1bar
phi2
phi2bar
GRESETbar
m-5
s-5
m-4
s-4
m-3
s-3
m-2
s-2
m-1
s-1
m0
s0
m1
s1
m2
s2
m3
s3
m4
s4
m5
s5
m6
s6
m7
s7
m8
s8
m9
x2jbar
x1jbar
x0jbar
&-2
&-1
&0
&1
&2
&3
&4
&5
&6
&7
D0bar
D1bar
D2bar
D3bar
D4bar
D5bar
D6bar
D7bar
D8bar
D0
D1
D2
D3
D4
D5
D6
D7
D8




3482 transistors, 1990 nodes (14 pulled up)
:phi1
:phi1bar
:phi2
:phi2bar
:ENABLE
:ENABLEbar
:GRESET
:GRESETbar
:m-6
:s-6
:m-5
:s-5
:m-4
:s-4
:m-3
:s-3
:m-2
:s-2
:m-1
:s-1
:m0
:s0
:m1
:s1
:m2
:s2
:m3
:s3
:m4
:s4
:m5
:s5
:m6
:s6
:m7
:s7
:m8
:s8
:m9
:s9
:m10
:s10
:m11
:s11
:out1
:out2
:out3
:out4
:out5
:out6
:out7
:out0
:$1
:$2
:$3
:$4
:$5
:$6
:$7
:$8
:$9
:$10
:$11
:$star1
:$star2

maui:faris

case8.out

Mon Dec 5 02:04:59 1988

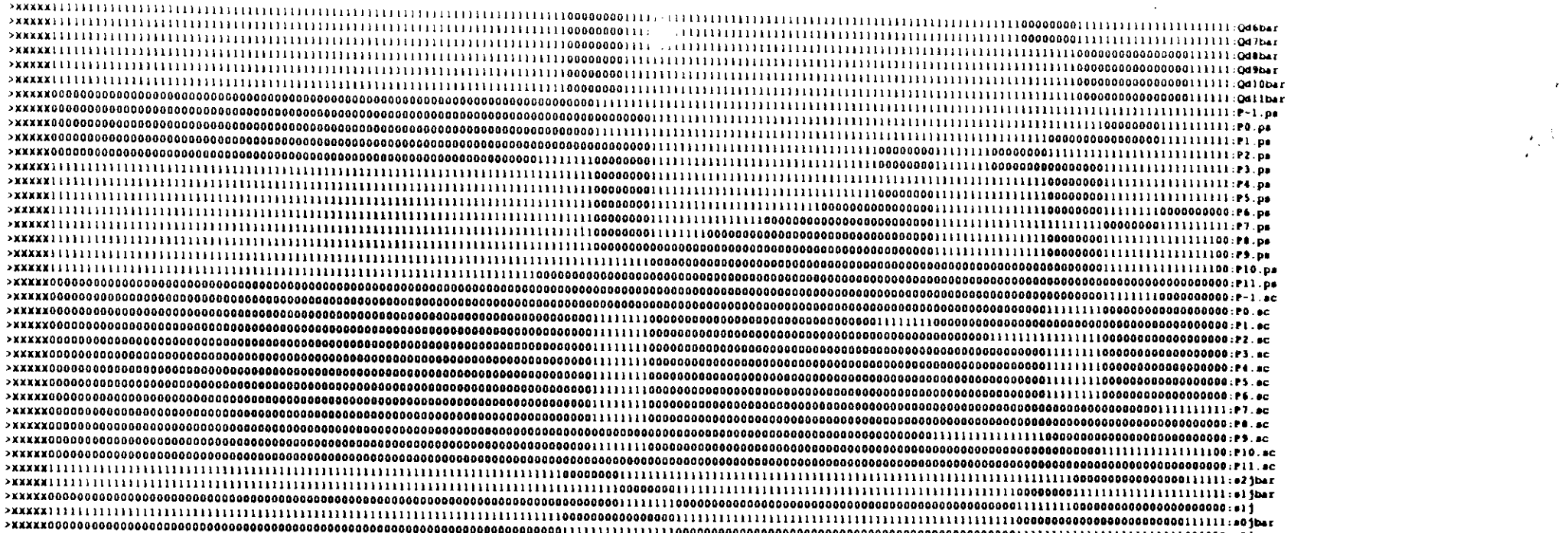
pub3 / Public 3

pub3 maui:faris Job: case8.out Date: Mon Dec 5 02:04:59 1988

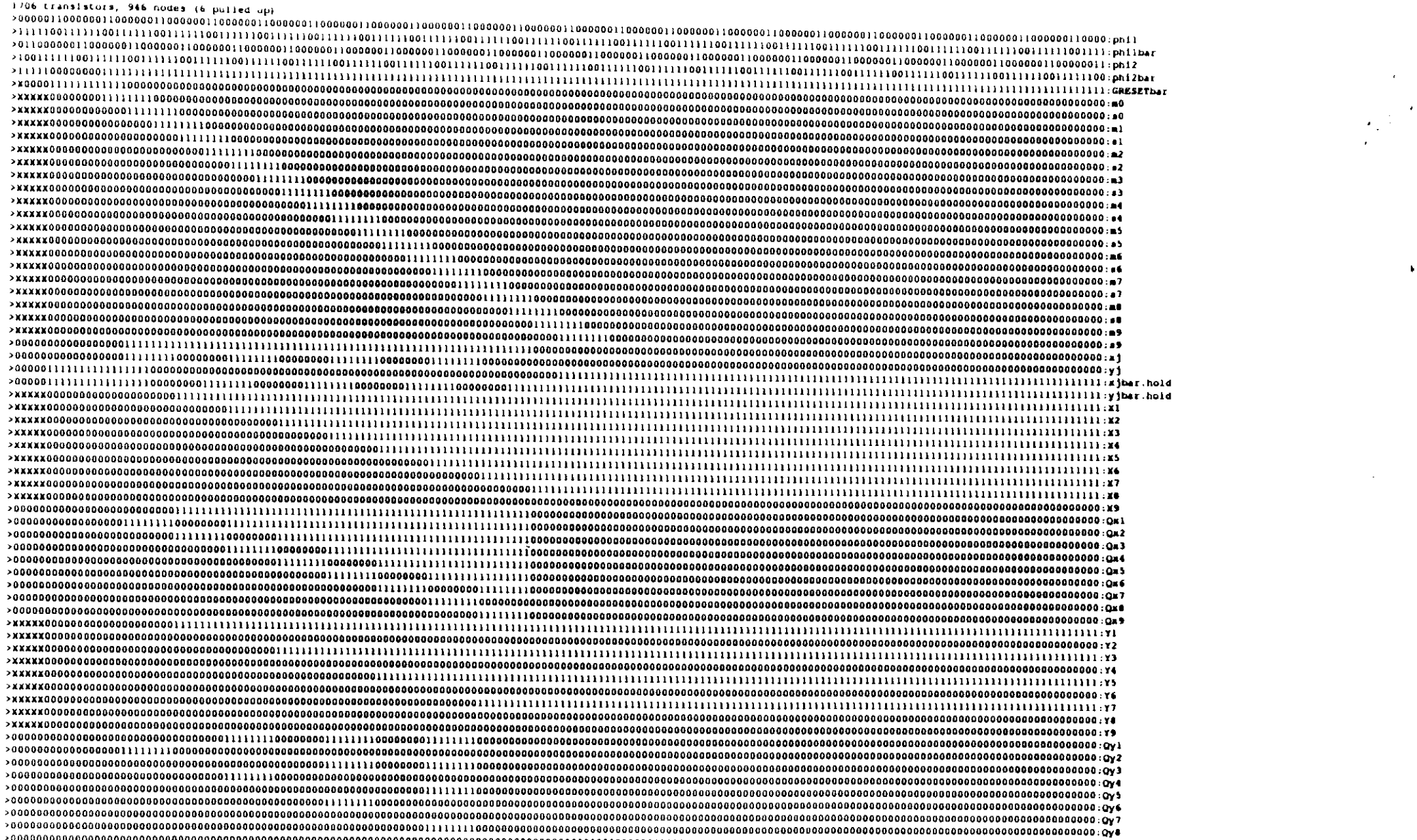
pub3 maui:faris Job: case8.out Date: Mon Dec 5 02:04:59 1988

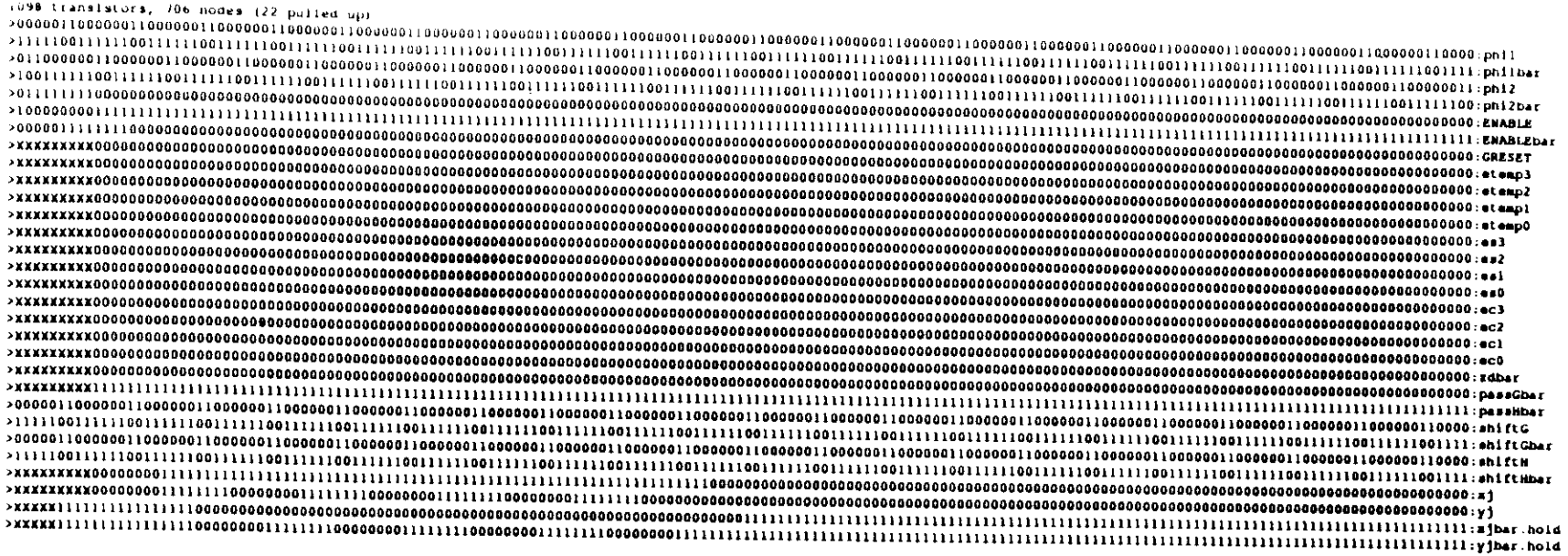
pub3 maui:faris Job: case8.out Date: Mon Dec 5 02:04:59 1988

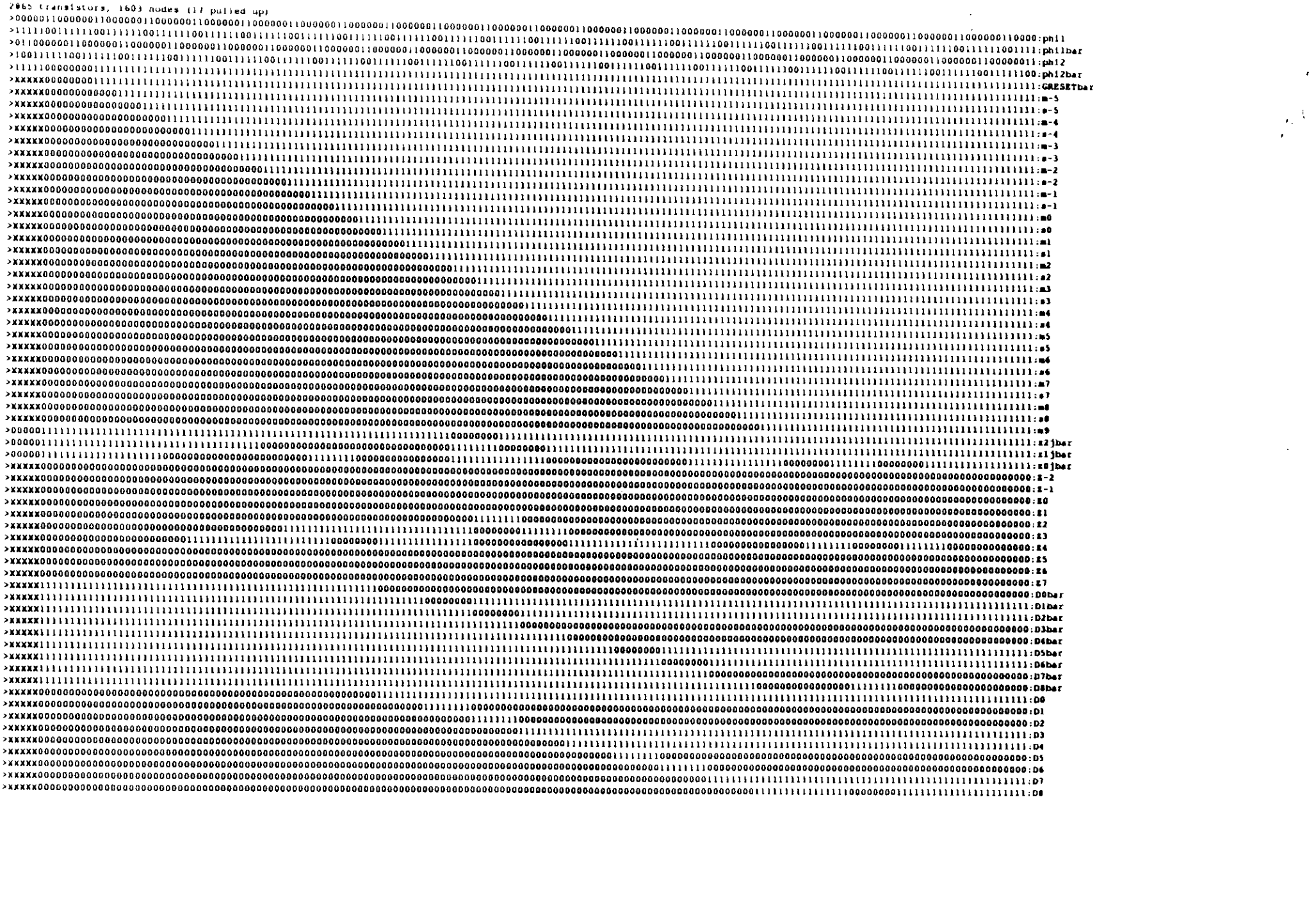
pub3 maui:faris Job: case8.out Date: Mon Dec 5 02:04:59 1988

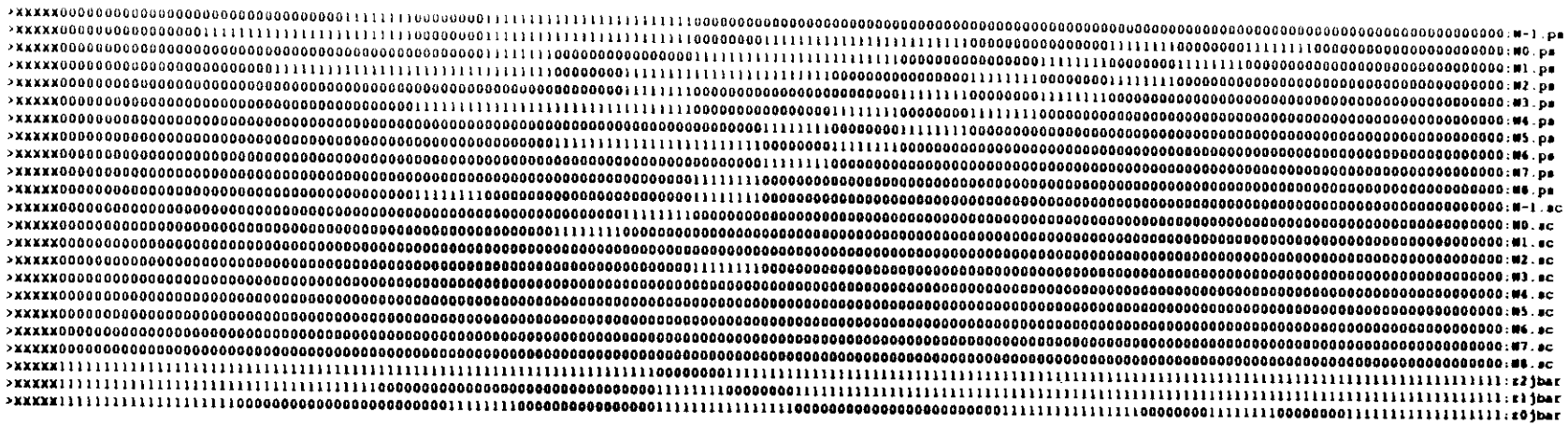

Qd6bar
Qd7bar
Qd8bar
Qd9bar
Qd10bar
Qd11bar
P-1.ps
P0.ps
P1.ps
P2.ps
P3.ps
P4.ps
P5.ps
P6.ps
P7.ps
P8.ps
P9.ps
P10.ps
P11.ps
P-1.sc
P0.sc
P1.sc
P2.sc
P3.sc
P4.sc
P5.sc
P6.sc
P7.sc
P8.sc
P9.sc
P10.sc
P11.sc
s2jbar
s1jbar
s1j
s0jbar
s0j

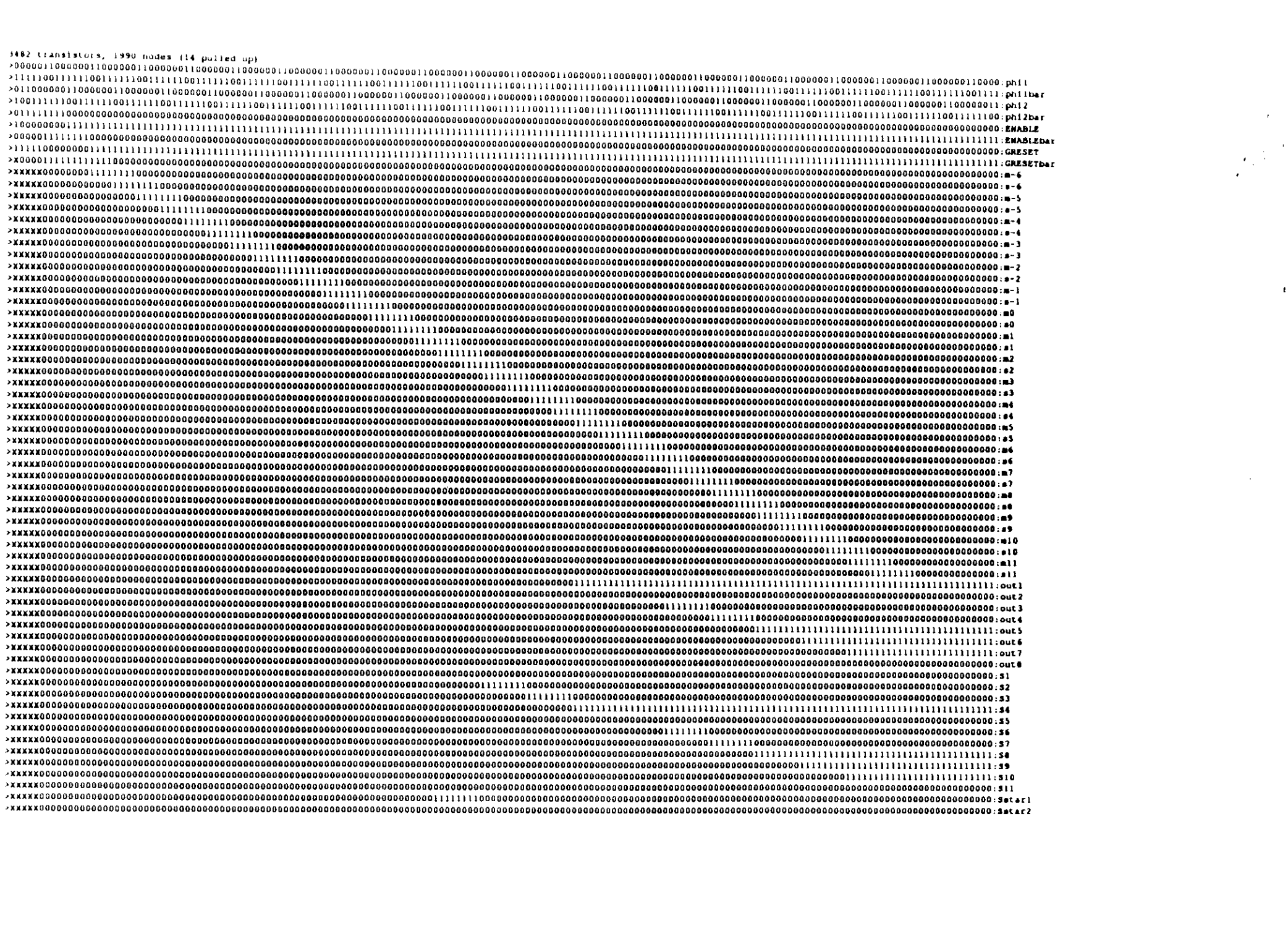
1706 transistors, 946 nodes (6 pulled up)

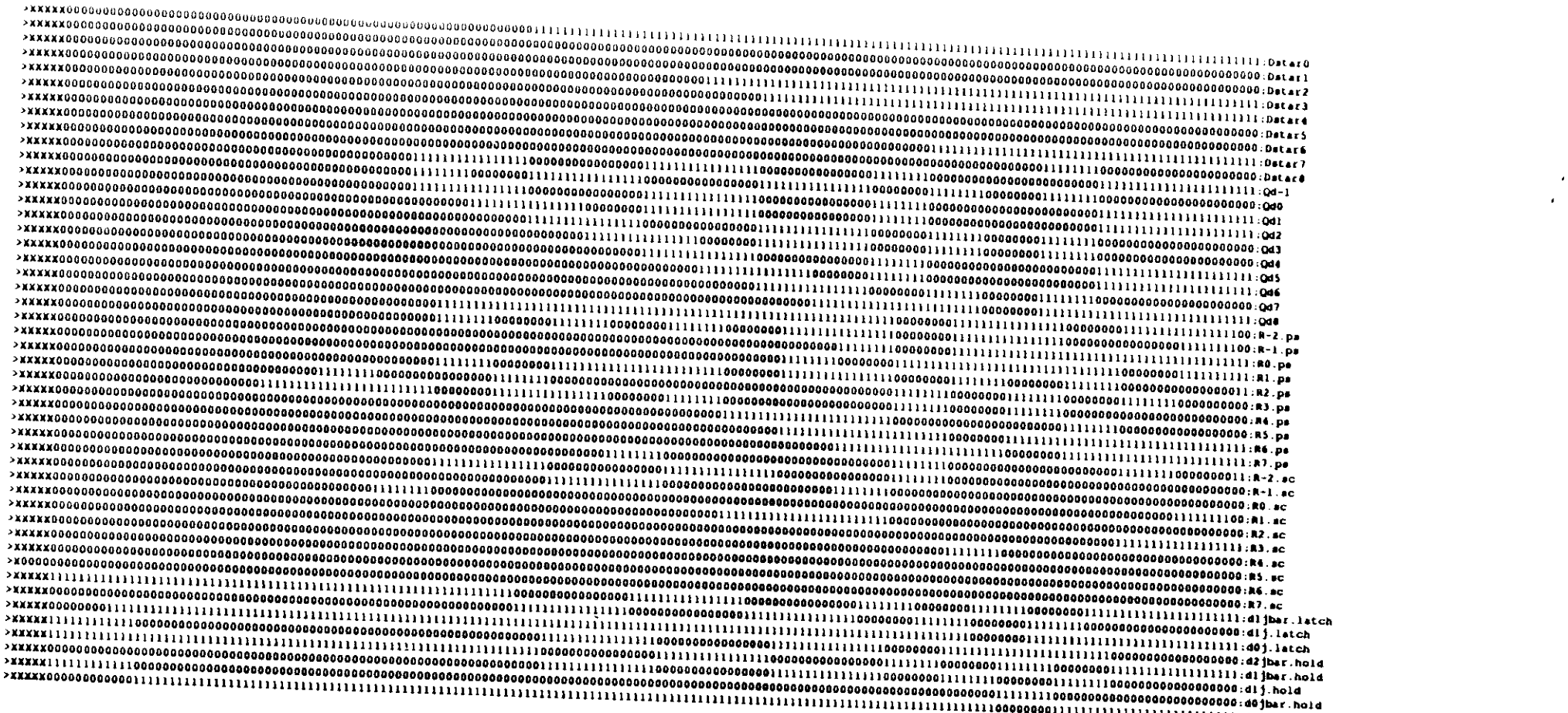


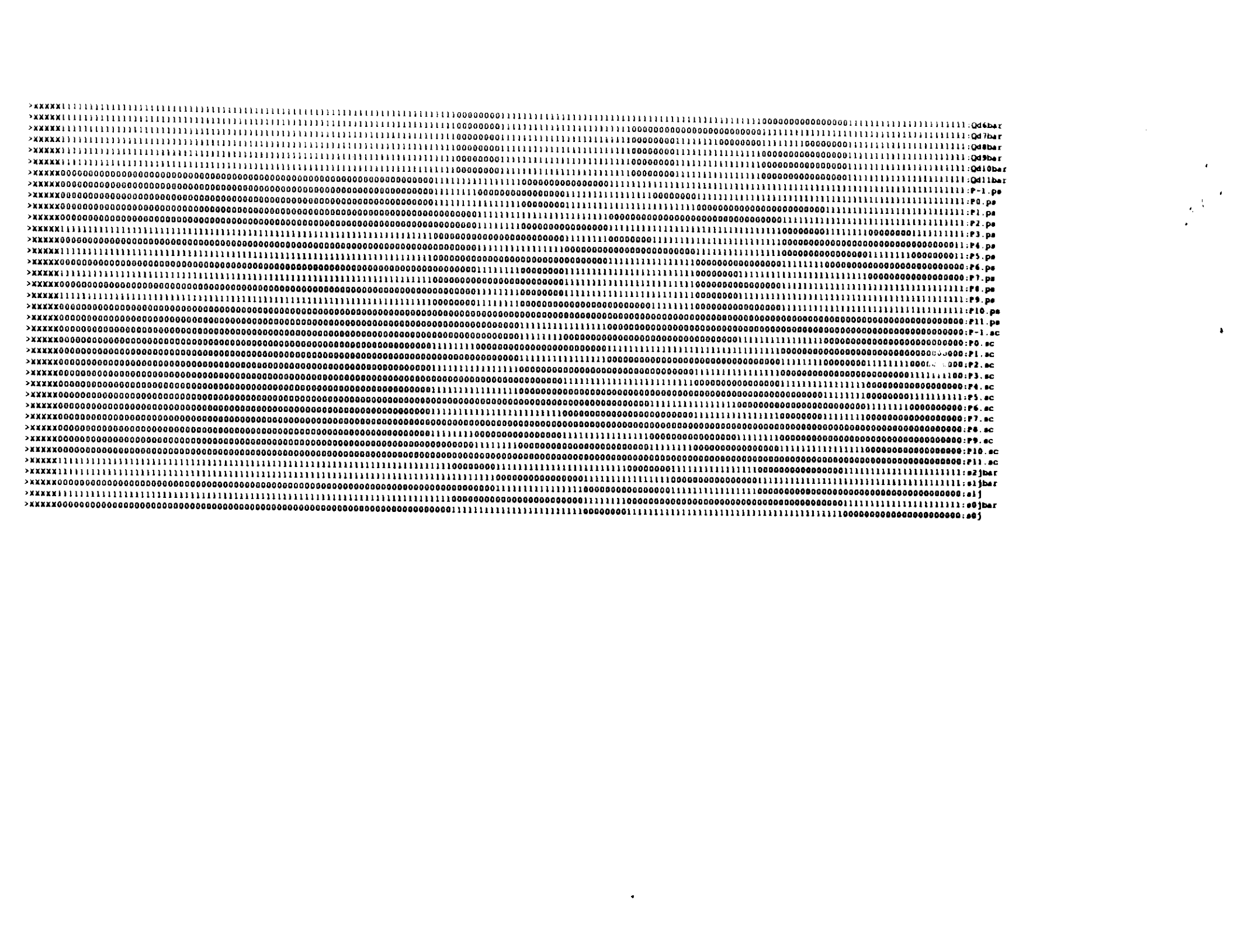

1098 transistors, 706 nodes (22 pulled up)
phi1
phi1bar
phi2
phi2bar
ENABLE
ENABLEbar
GRESET
etemp3
etemp2
etemp1
etemp0
es3
es2
es1
es0
ec3
ec2
ec1
ec0
rdbar
passGbar
passHbar
shiftG
shiftGbar
shiftH
shiftHbar
xj
yj
xjbar.hold
yjbar.hold

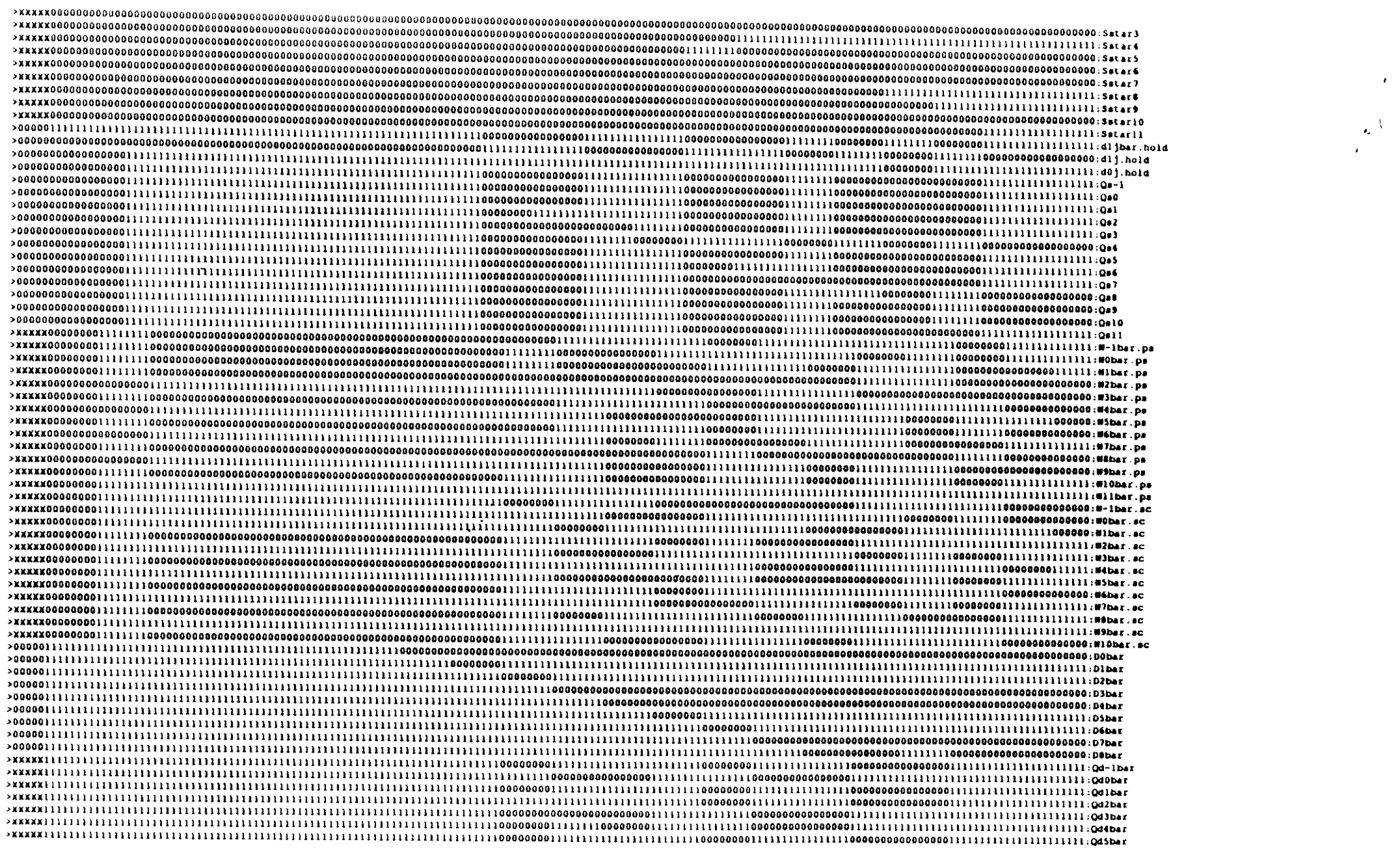

2065 transistors, 1603 nodes (17 pulled up)
:ph11
:ph11bar
:ph12
:ph12bar
:GRESETbar
:m-5
:s-5
:m-4
:s-4
:m-3
:s-3
:m-2
:s-2
:m-1
:s-1
:m0
:s0
:m1
:s1
:m2
:s2
:m3
:s3
:m4
:s4
:m5
:s5
:m6
:s6
:m7
:s7
:m8
:s8
:m9
:s2jbar
:s1jbar
:s0jbar
:s-2
:s-1
:s0
:s1
:s2
:s3
:s4
:s5
:s6
:s7
:D0bar
:D1bar
:D2bar
:D3bar
:D4bar
:D5bar
:D6bar
:D7bar
:D8bar
:D0
:D1
:D2
:D3
:D4
:D5
:D6
:D7
:D8


M-1.ps
M0.ps
M1.ps
M2.ps
M3.ps
M4.ps
M5.ps
M6.ps
M7.ps
M8.ps
M-1.sc
M0.sc
M1.sc
M2.sc
M3.sc
M4.sc
M5.sc
M6.sc
M7.sc
M8.sc
z2jbar
z1jbar
z0jbar


3482 transistors, 1990 nodes (114 pulled up)
:ph11
:ph11bar
:ph12
:ph12bar
:ENABLE
:ENABLEbar
:GRESET
:GRESETbar
:m-6
:s-6
:m-5
:s-5
:m-4
:s-4
:m-3
:s-3
:m-2
:s-2
:m-1
:s-1
:m0
:s0
:m1
:s1
:m2
:s2
:m3
:s3
:m4
:s4
:m5
:s5
:m6
:s6
:m7
:s7
:m8
:s8
:m9
:s9
:m10
:s10
:m11
:s11
:out1
:out2
:out3
:out4
:out5
:out6
:out7
:out8
:$1
:$2
:$3
:$4
:$5
:$6
:$7
:$8
:$9
:$10
:$11
:$star1
:$star2


:Dstar0
:Dstar1
:Dstar2
:Dstar3
:Dstar4
:Dstar5
:Dstar6
:Dstar7
:Dstar8
:Qd-1
:Qd0
:Qd1
:Qd2
:Qd3
:Qd4
:Qd5
:Qd6
:Qd7
:Qd8
:R-2.ps
:R-1.ps
:R0.ps
:R1.ps
:R2.ps
:R3.ps
:R4.ps
:R5.ps
:R6.ps
:R7.ps
:R-2.sc
:R-1.sc
:R0.sc
:R1.sc
:R2.sc
:R3.sc
:R4.sc
:R5.sc
:R6.sc
:R7.sc
:dljbar.latch
:dlj.latch
:d0j.latch
:d2jbar.hold
:dljbar.hold
:dlj.hold
:d0jbar.hold
:d0j.hold





maui:faris

case1.out

Thu Dec 15 00:05:42 1988

pub3 / Public 3

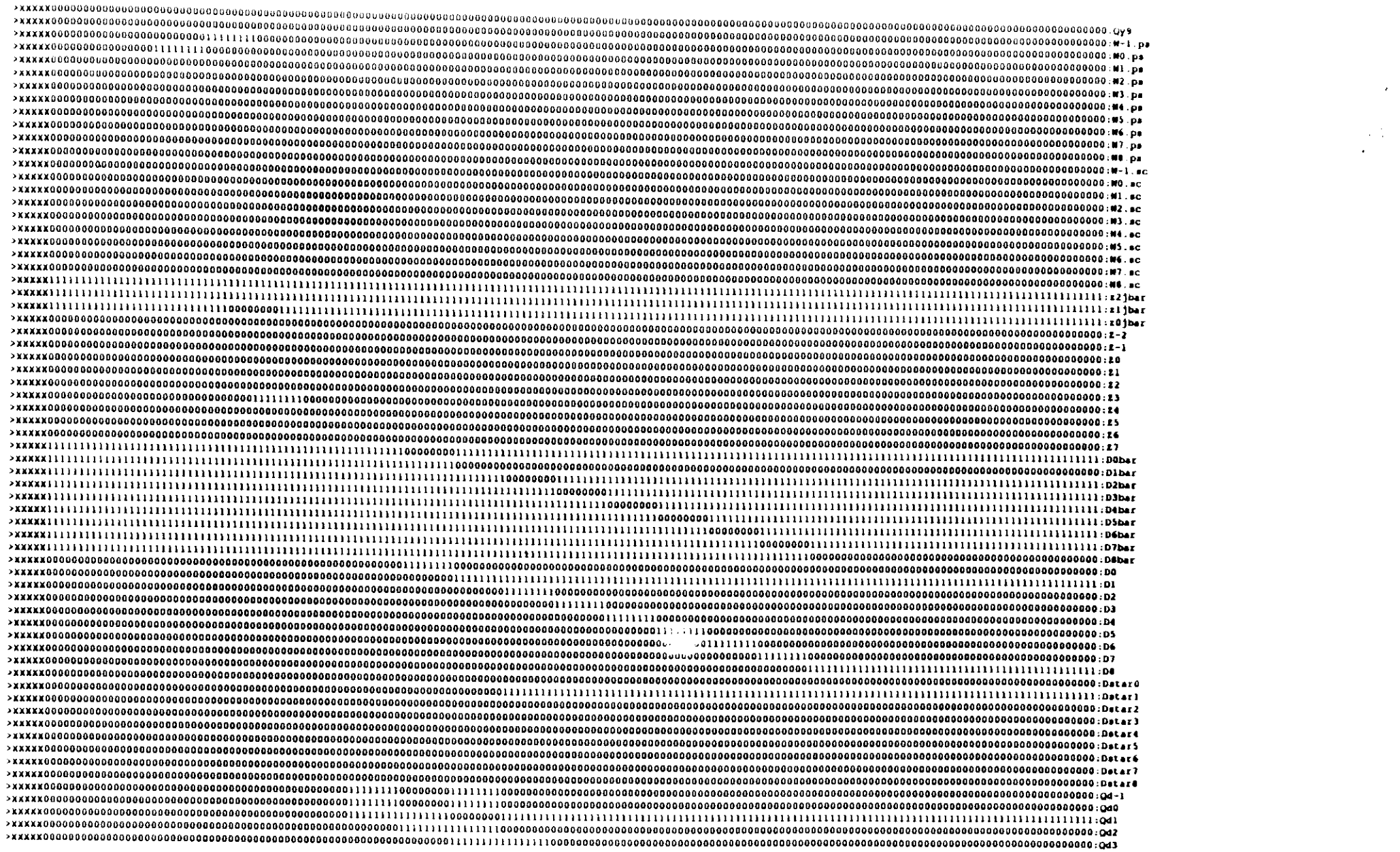
pub3 maui:faris Job: case1.out Date: Thu Dec 15 00:05:42 1988

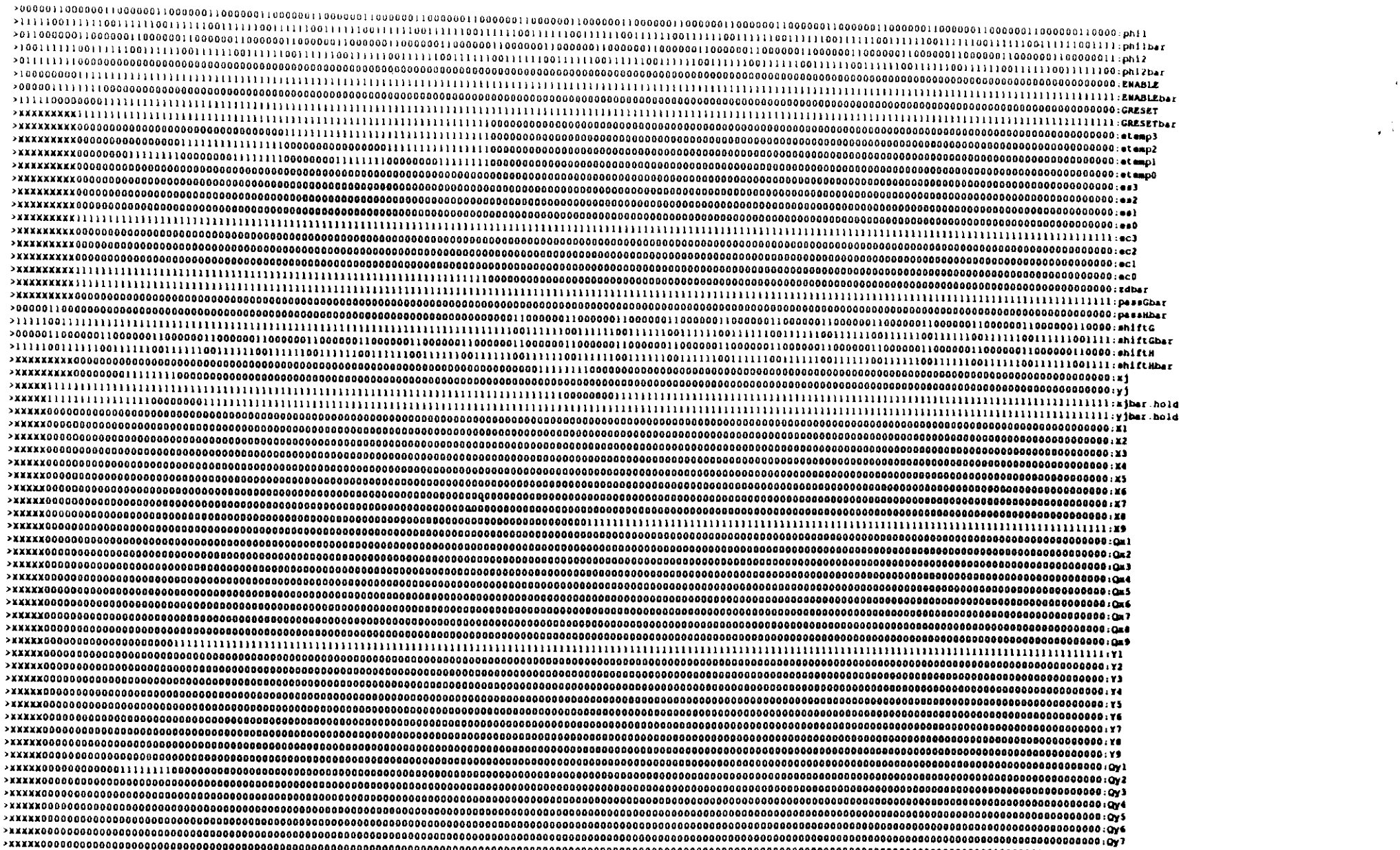
pub3 maui:faris Job: case1.out Date: Thu Dec 15 00:05:42 1988

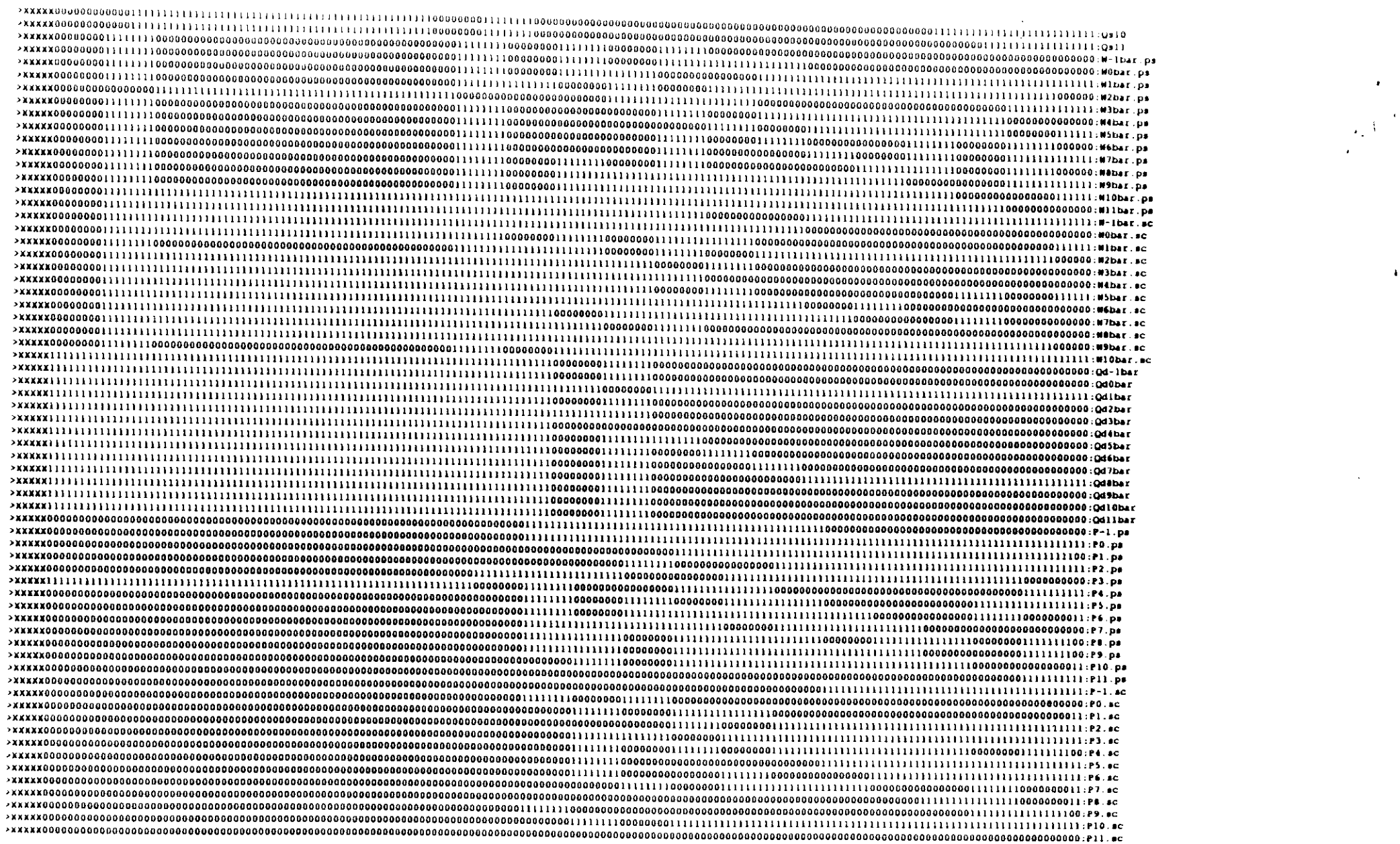
pub3 maui:faris Job: case1.out Date: Thu Dec 15 00:05:42 1988

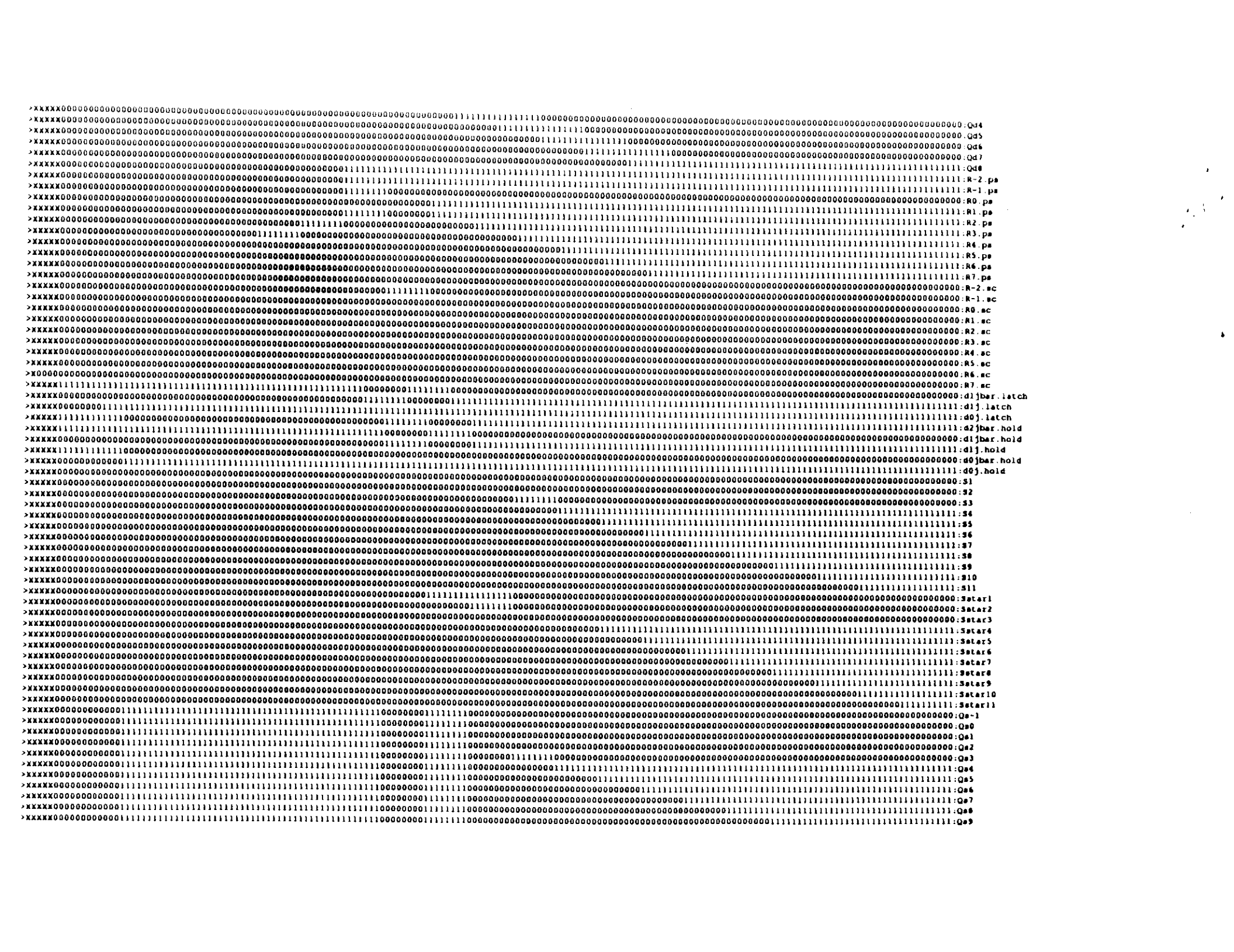
pub3 maui:faris Job: case1.out Date: Thu Dec 15 00:05:42 1988

1.2 Esim Results: Final (Chip-wide, Cases #1 - #12)


Qy9
W-1.ps
W0.ps
W1.ps
W2.ps
W3.ps
W4.ps
W5.ps
W6.ps
W7.ps
W8.ps
W-1.sc
W0.sc
W1.sc
W2.sc
W3.sc
W4.sc
W5.sc
W6.sc
W7.sc
W8.sc
z2jbar
z1jbar
z0jbar
Z-2
Z-1
Z0
Z1
Z2
Z3
Z4
Z5
Z6
Z7
D0bar
D1bar
D2bar
D3bar
D4bar
D5bar
D6bar
D7bar
D8bar
D0
D1
D2
D3
D4
D5
D6
D7
D8
Datar0
Datar1
Datar2
Datar3
Datar4
Datar5
Datar6
Datar7
Datar8
Qd-1
Qd0
Qd1
Qd2
Qd3


phi1
phi1bar
phi2
phi2bar
ENABLE
ENABLEbar
GRESET
GRESETbar
etemp3
etemp2
etemp1
etemp0
es3
es2
es1
es0
ec3
ec2
ec1
ec0
rdbar
passGbar
passHbar
shiftG
shiftGbar
shiftH
shiftHbar
xj
yj
xjbar.hold
yjbar.hold
X1
X2
X3
X4
X5
X6
X7
X8
X9
Qx1
Qx2
Qx3
Qx4
Qx5
Qx6
Qx7
Qx8
Qx9
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
Qy1
Qy2
Qy3
Qy4
Qy5
Qy6
Qy7
Qy8





maui:faris

case2.out

Thu Dec 15 00:08:27 1988

pub3 / Public 3

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pub3 maui:faris  Job: case2.out  Date: Thu Dec 15 00:08:27 1988

pub3 maui:faris  Job: case2.out  Date: Thu Dec 15 00:08:27 1988

pub3 maui:faris  Job: case2.out  Date: Thu Dec 15 00:08:27 1988

pub3 maui:faris  Job: case2.out  Date: Thu Dec 15 00:08:27 1988
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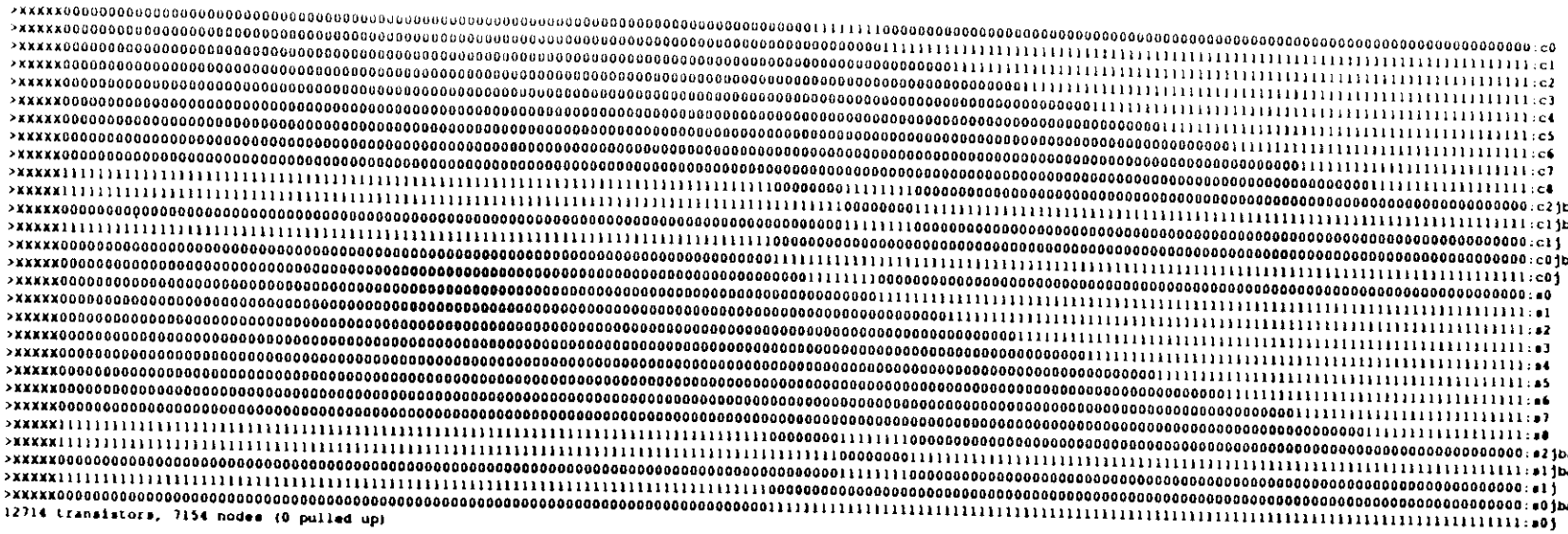
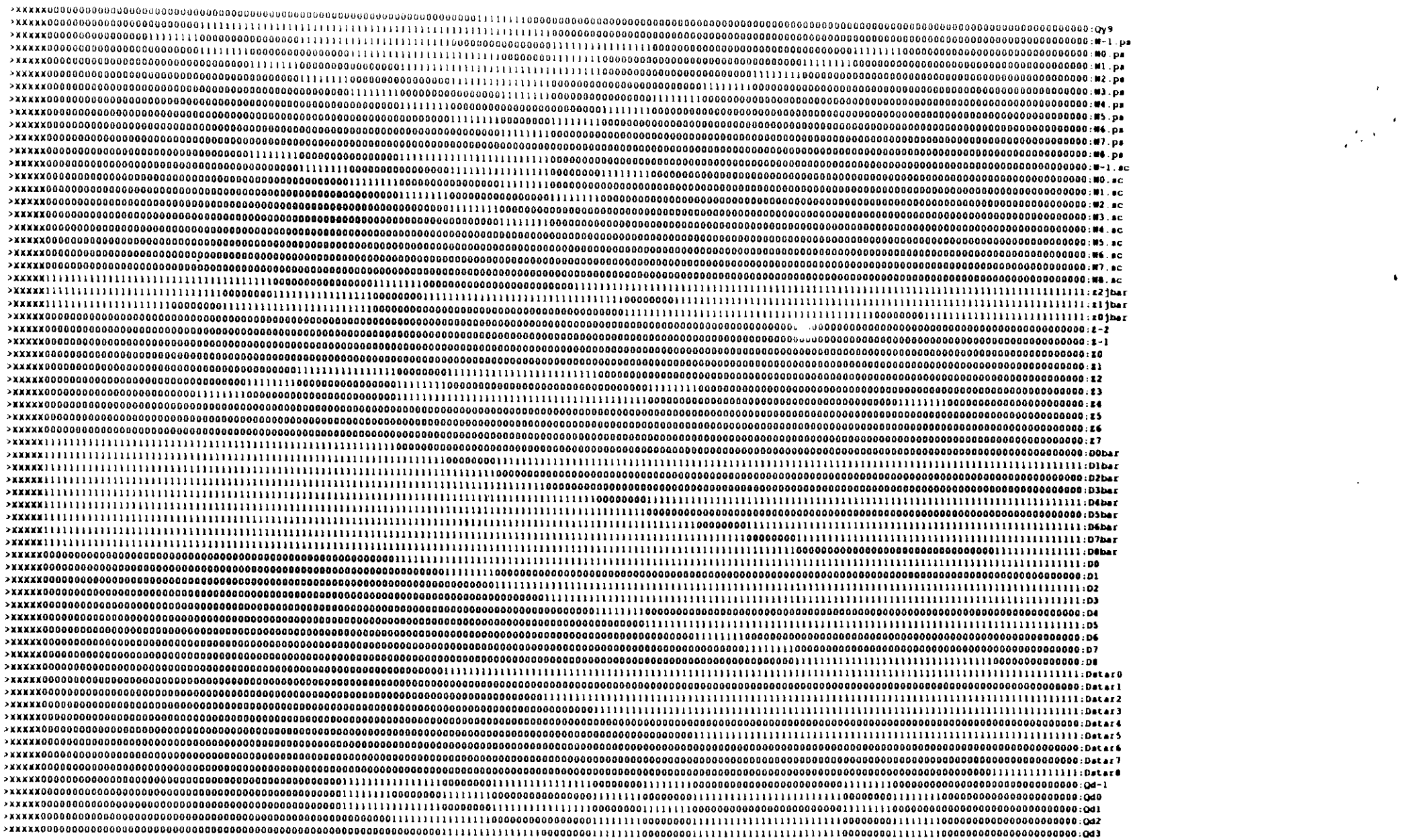
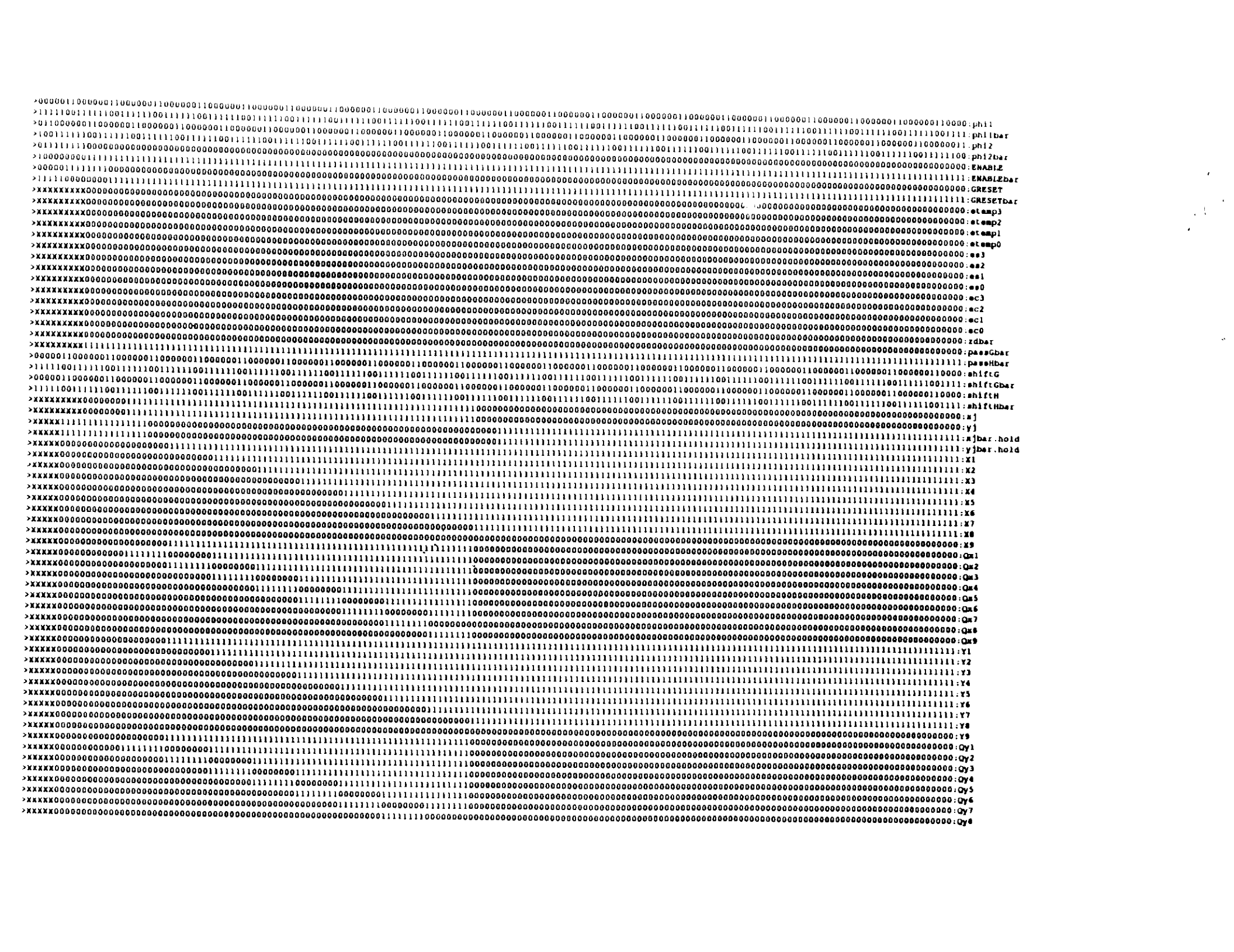
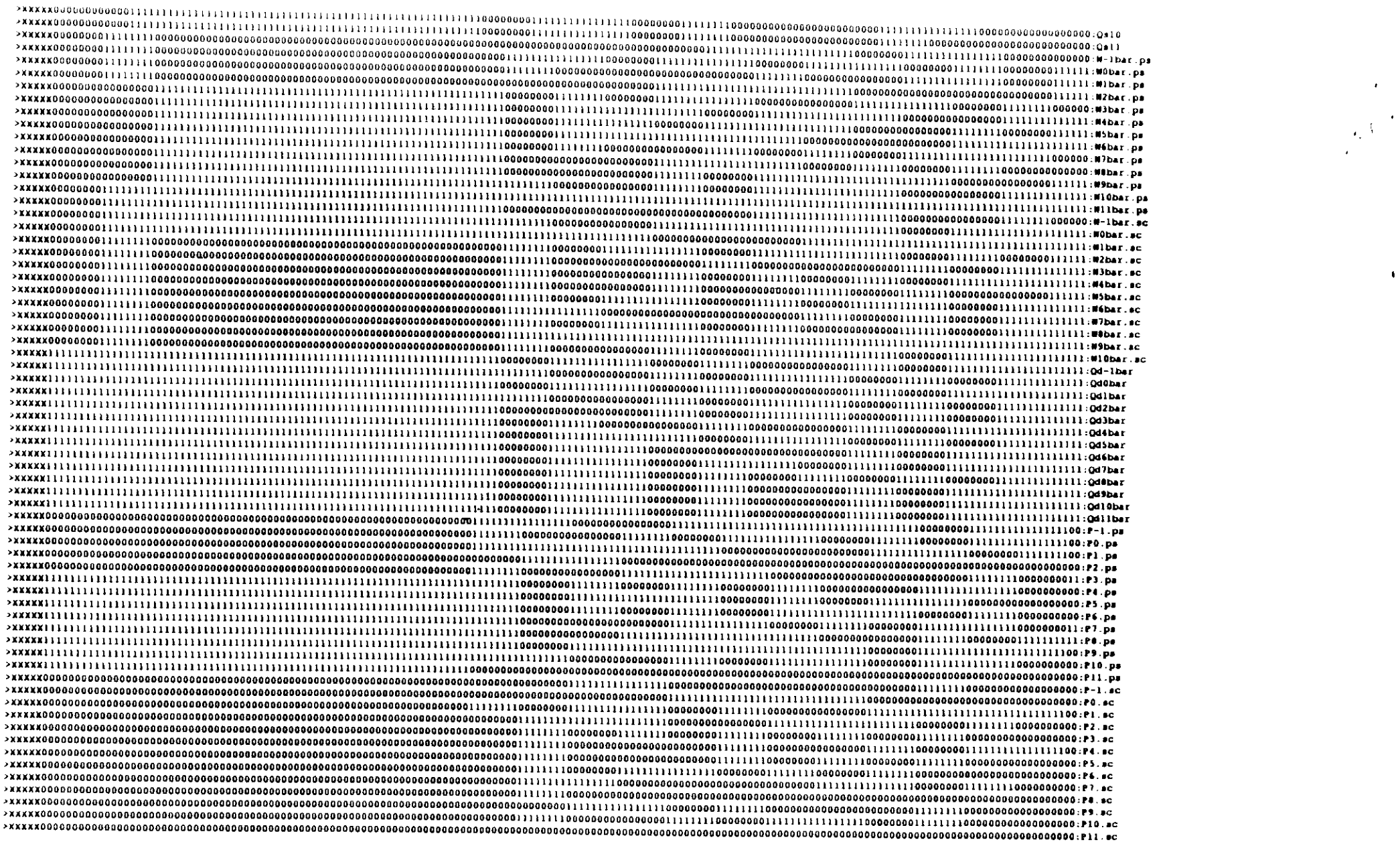
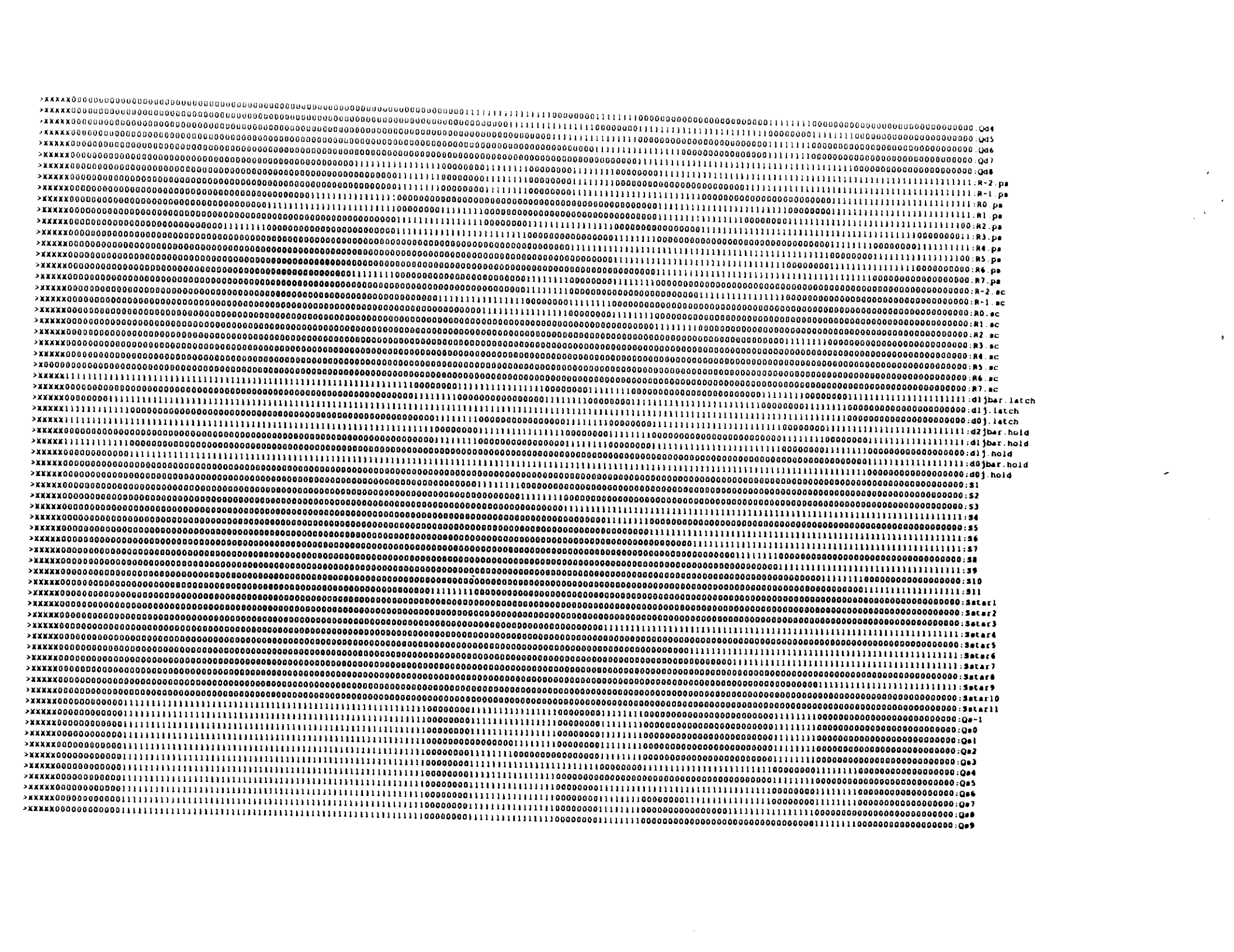


12714 transistors, 7154 nodes (0 pulled up)









maui:faris

case3.out

Thu Dec 15 00:10:49 1988

pub3 / Public 3

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pub3 maui:faris  Job: case3.out  Date: Thu Dec 15 00:10:49 1988

pub3 maui:faris  Job: case3.out  Date: Thu Dec 15 00:10:49 1988

pub3 maui:faris  Job: case3.out  Date: Thu Dec 15 00:10:49 1988

pub3 maui:faris  Job: case3.out  Date: Thu Dec 15 00:10:49 1988
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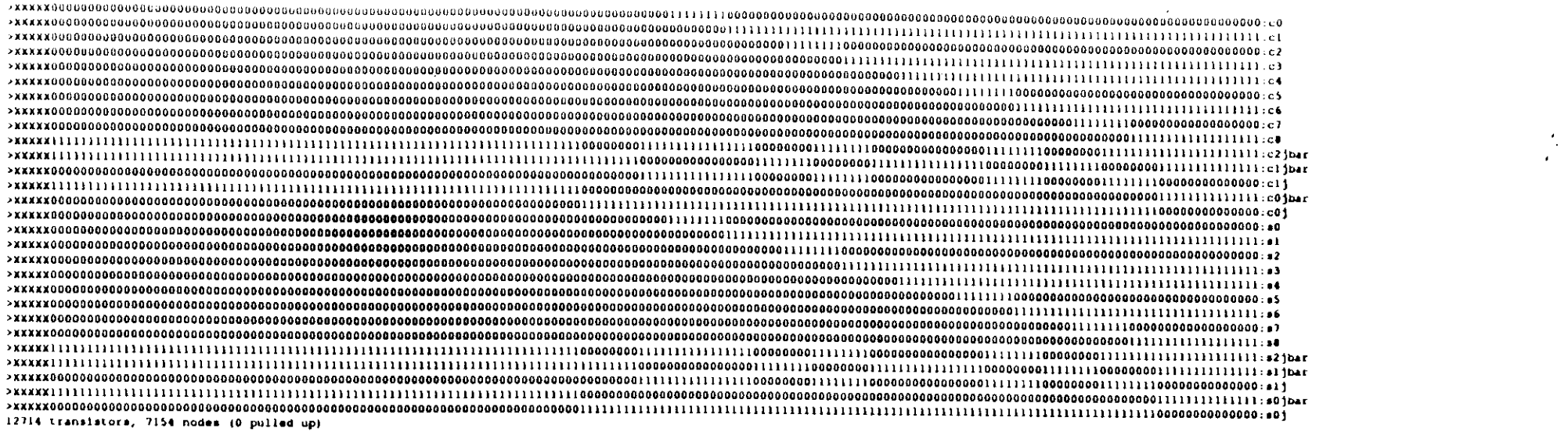
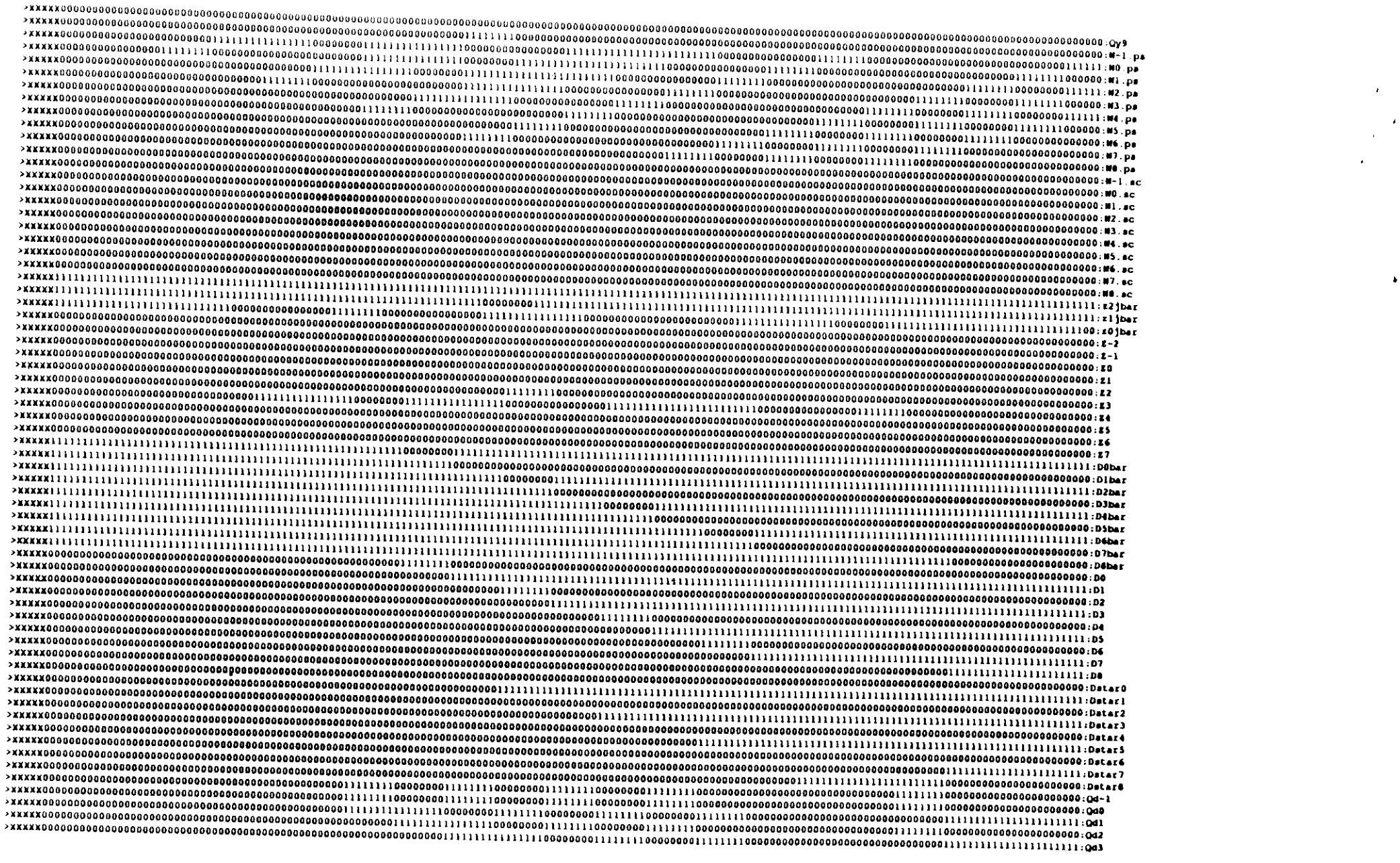


12714 translators, 7154 nodes (0 pulled up)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:M-1.ps
:M0.ps
:M1.ps
:M2.ps
:M3.ps
:M4.ps
:M5.ps
:M6.ps
:M7.ps
:M8.ps
:M-1.sc
:M0.sc
:M1.sc
:M2.sc
:M3.sc
:M4.sc
:M5.sc
:M6.sc
:M7.sc
:M8.sc
:z2jbar
:z1jbar
:z0jbar
:Z-2
:Z-1
:Z0
:Z1
:Z2
:Z3
:Z4
:Z5
:Z6
:Z7
:D0bar
:D1bar
:D2bar
:D3bar
:D4bar
:D5bar
:D6bar
:D7bar
:D8bar
:D0
:D1
:D2
:D3
:D4
:D5
:D6
:D7
:D8
:Dstar0
:Dstar1
:Dstar2
:Dstar3
:Dstar4
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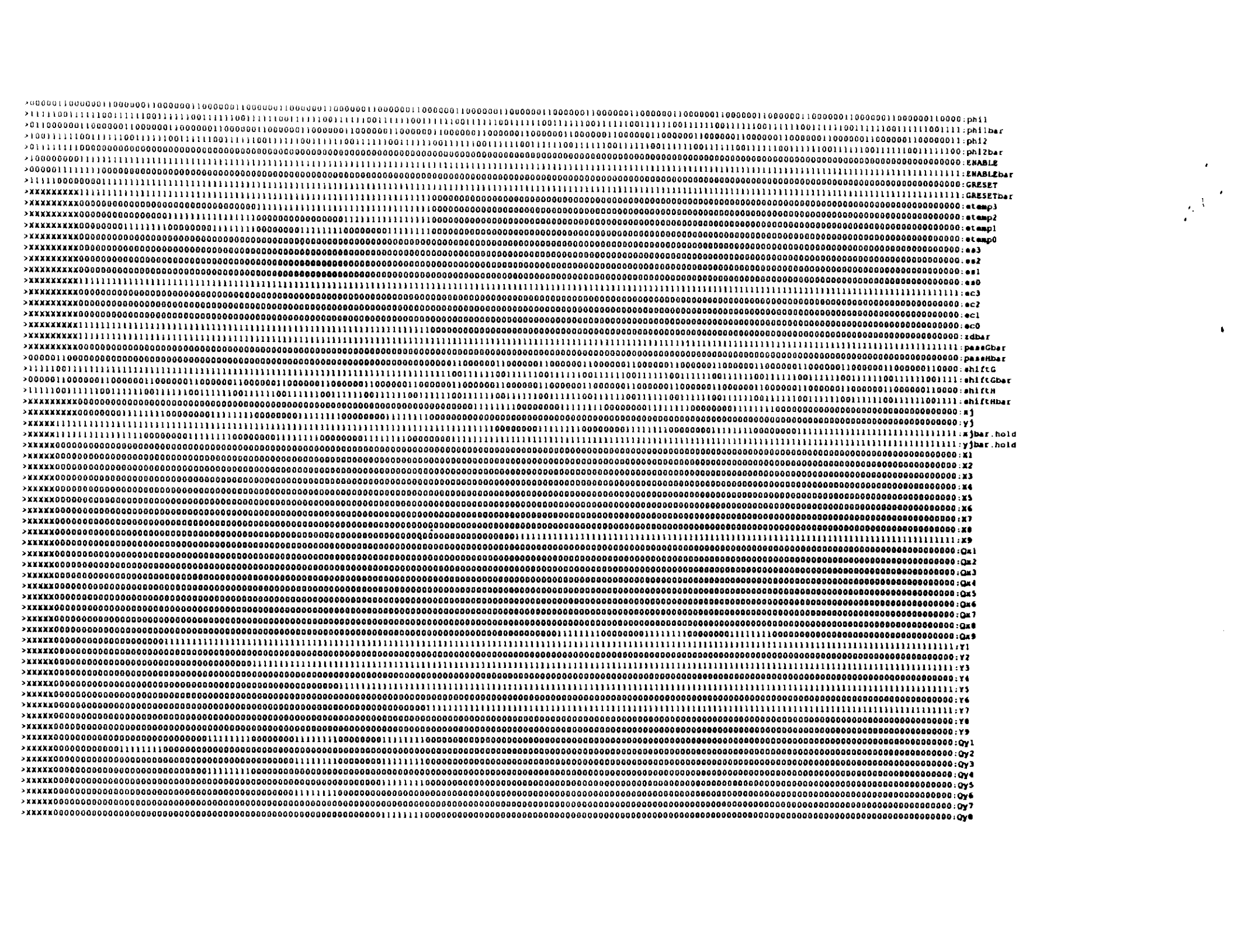
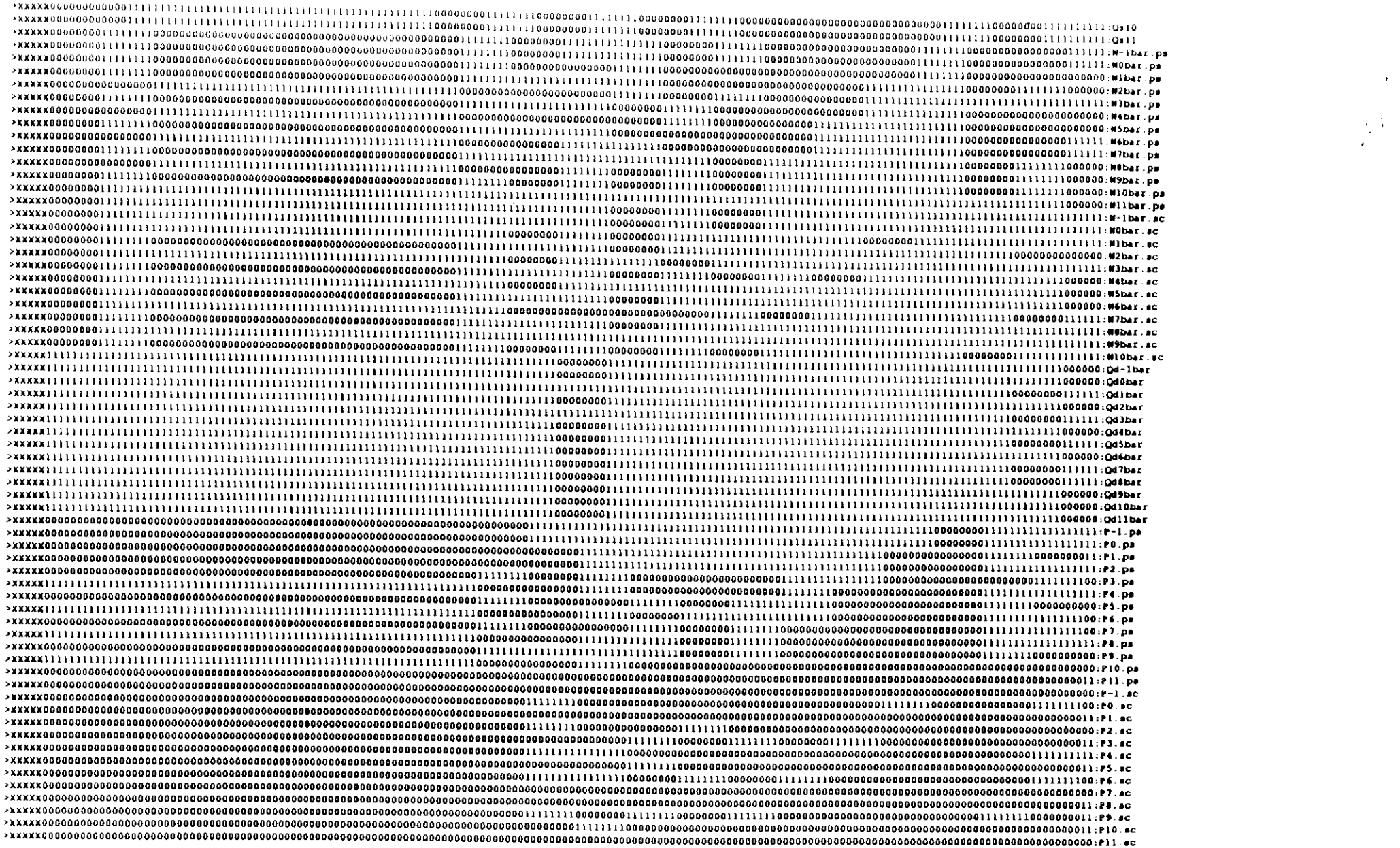
:Dstar6
:Dstar7
:Dstar8
:Qd-1
:Qd0
:Qd1
:Qd2
:Qd3




Qs10
Qs11
W-1bar.ps
W0bar.ps
W1bar.ps
W2bar.ps
W3bar.ps
W4bar.ps
W5bar.ps
W6bar.ps
W7bar.ps
W8bar.ps
W9bar.ps
W10bar.ps
W11bar.ps
W-1bar.sc
W0bar.sc
W1bar.sc
W2bar.sc
W3bar.sc
W4bar.sc
W5bar.sc
W6bar.sc
W7bar.sc
W8bar.sc
W9bar.sc
W10bar.sc
Qd-1bar
Qd0bar
Qd1bar
Qd2bar
Qd3bar
Qd4bar
Qd5bar
Qd6bar
Qd7bar
Qd8bar
Qd9bar
Qd10bar
Qd11bar
P-1.ps
P0.ps
P1.ps
P2.ps
P3.ps
P4.ps
P5.ps
P6.ps
P7.ps
P8.ps
P9.ps
P10.ps
P11.ps
P-1.sc
P0.sc
P1.sc
P2.sc
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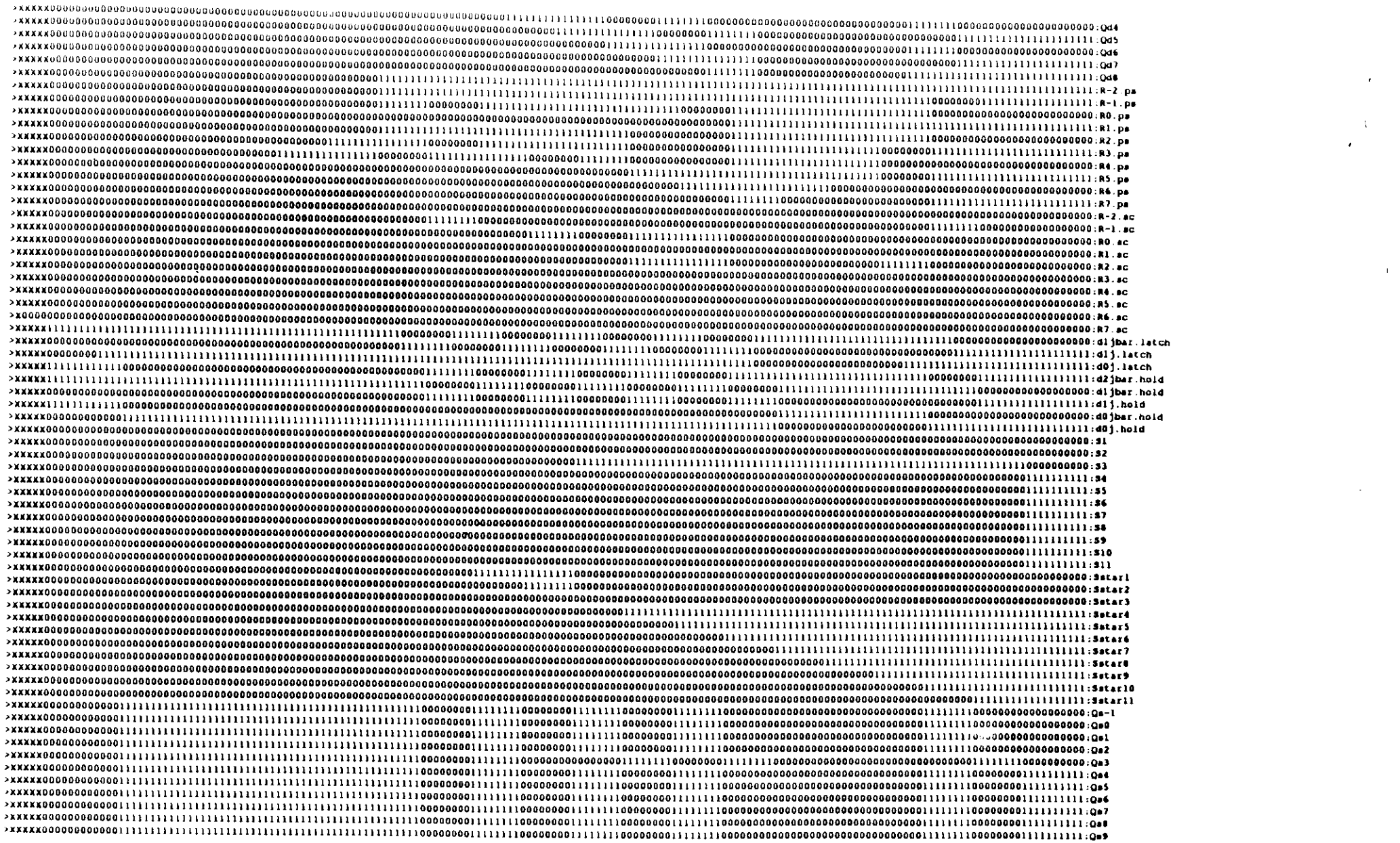
P4.sc
P5.sc
P6.sc
P7.sc
P8.sc
P9.sc
P10.sc
P11.sc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Qd5
Qd6
Qd7
Qd8
R-2.ps
R-1.ps
R0.ps
R1.ps
R2.ps
R3.ps
R4.ps
R5.ps
R6.ps
R7.ps
R-2.sc
R-1.sc
R0.sc
R1.sc
R2.sc
R3.sc
R4.sc
R5.sc
R6.sc
R7.sc
d1jbar.latch
d1j.latch
d0j.latch
d2jbar.hold
d1jbar.hold
d1j.hold
d0jbar.hold
d0j.hold
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
Sstar1
Sstar2
Sstar3
Sstar4
Sstar5
Sstar6
Sstar7
Sstar8
Sstar9
Sstar10
Sstar11
Qs-1
Qs0
Qs1
Qs2
Qs3
Qs4
Qs5
Qs6
Qs7
Qs8
Qs9

maui:faris

case4.out

Thu Dec 15 00:13:11 1988

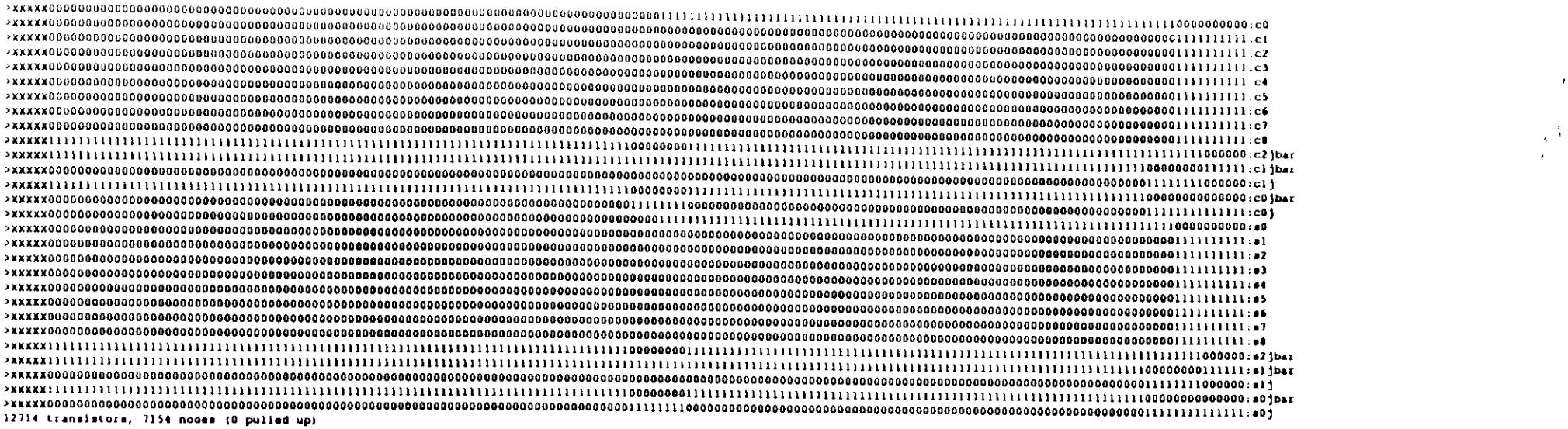
pub3 / Public 3

pub3 maui:faris Job: case4.out Date: Thu Dec 15 00:13:11 1988

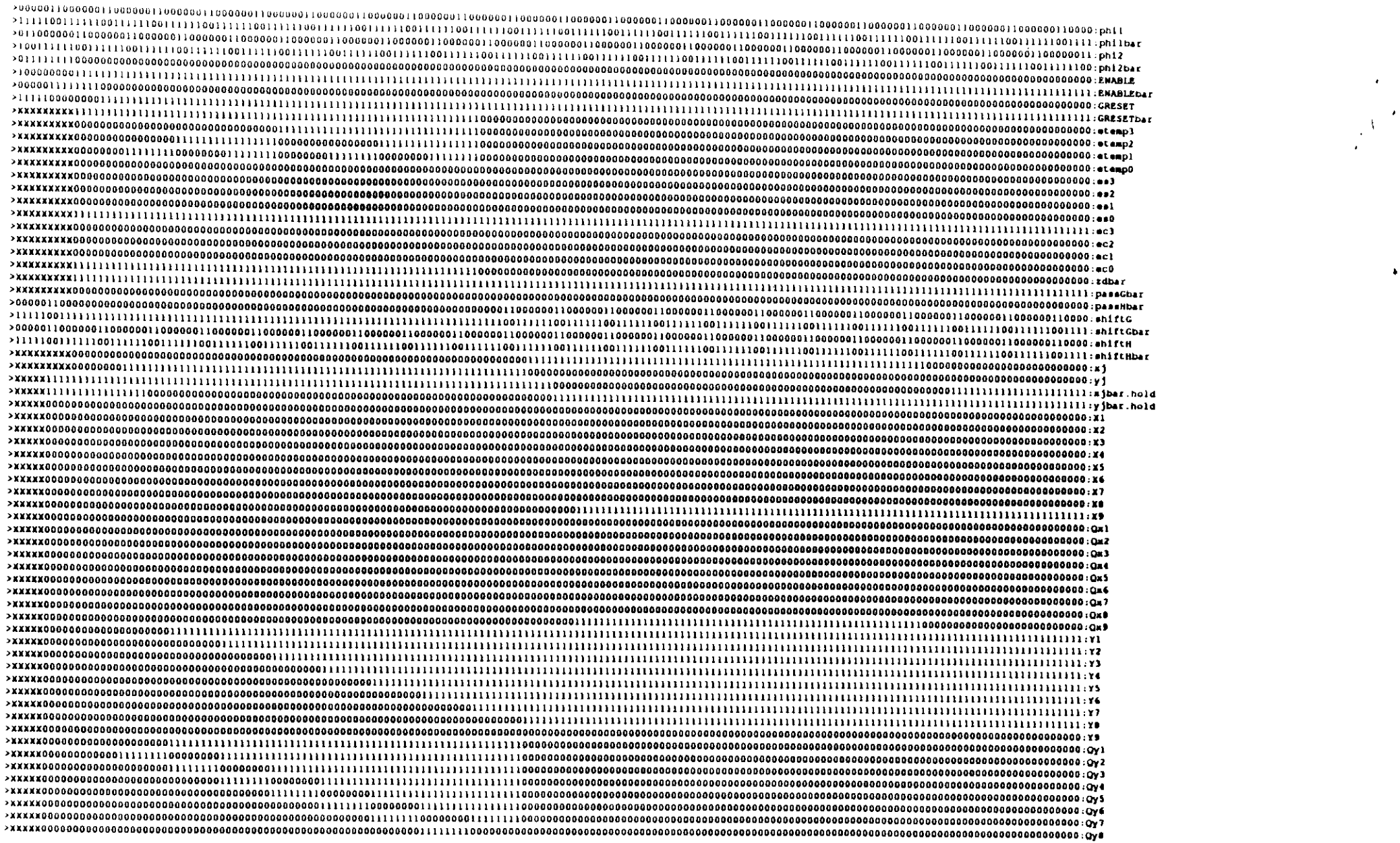
pub3 maui:faris Job: case4.out Date: Thu Dec 15 00:13:11 1988

pub3 maui:faris Job: case4.out Date: Thu Dec 15 00:13:11 1988

pub3 maui:faris Job: case4.out Date: Thu Dec 15 00:13:11 1988



12714 transistors, 7154 nodes (0 pulled up)


phi1
phi1bar
phi2
phi2bar
ENABLE
ENABLEbar
GRESET
GRESETbar
etemp3
etemp2
etemp1
etemp0
es3
es2
es1
es0
ec3
ec2
ec1
ec0
zdbar
passGbar
passHbar
shiftG
shiftGbar
shiftH
shiftHbar
xj
yj
xjbar.hold
yjbar.hold
X1
X2
X3
X4
X5
X6
X7
X8
X9
Qx1
Qx2
Qx3
Qx4
Qx5
Qx6
Qx7
Qx8
Qx9
Y1
Y2
Y3
Y4
Y5
Y6
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Y8
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Qy3
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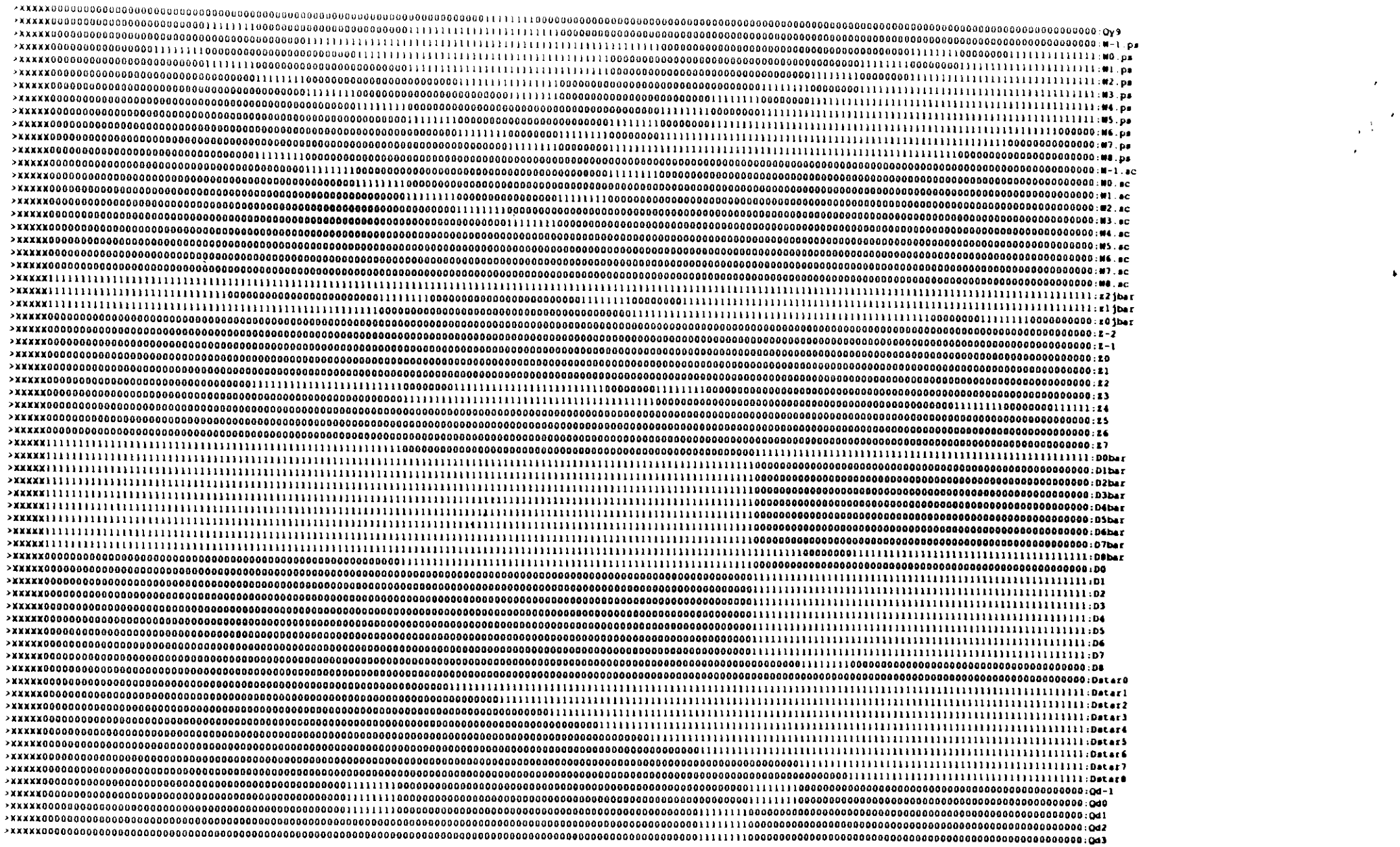
Qy5
Qy6
Qy7
Qy8


Qy9
W-1.ps
W0.ps
W1.ps
W2.ps
W3.ps
W4.ps
W5.ps
W6.ps
W7.ps
W8.ps
W-1.ac
W0.ac
W1.ac
W2.ac
W3.ac
W4.ac
W5.ac
W6.ac
W7.ac
W8.ac
z2jbar
z1jbar
z0jbar
Z-2
Z-1
Z0
Z1
Z2
Z3
Z4
Z5
Z6
Z7
D0bar
D1bar
D2bar
D3bar
D4bar
D5bar
D6bar
D7bar
D8bar
D0
D1
D2
D3
D4
D5
D6
D7
D8
Dstar0
Dstar1
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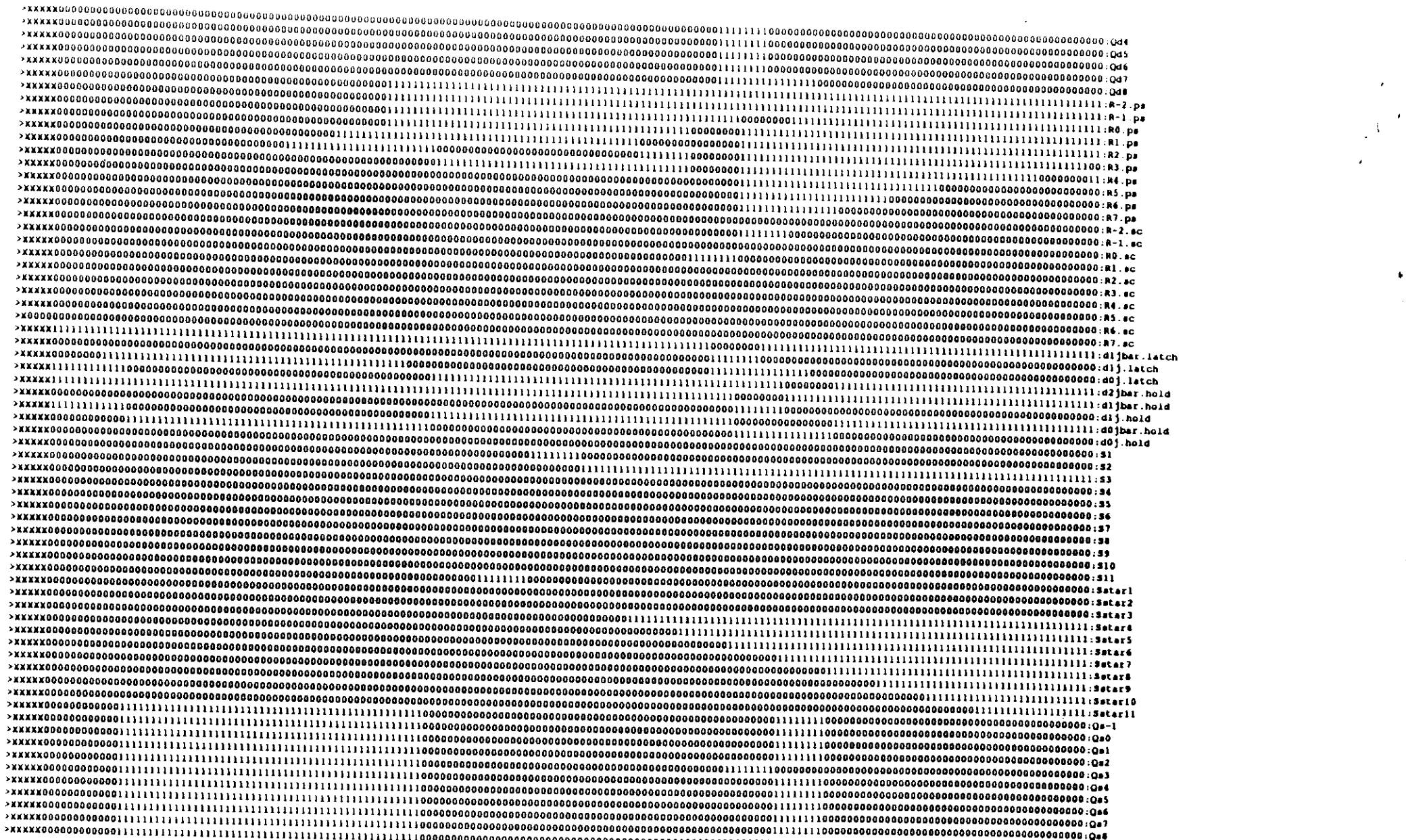
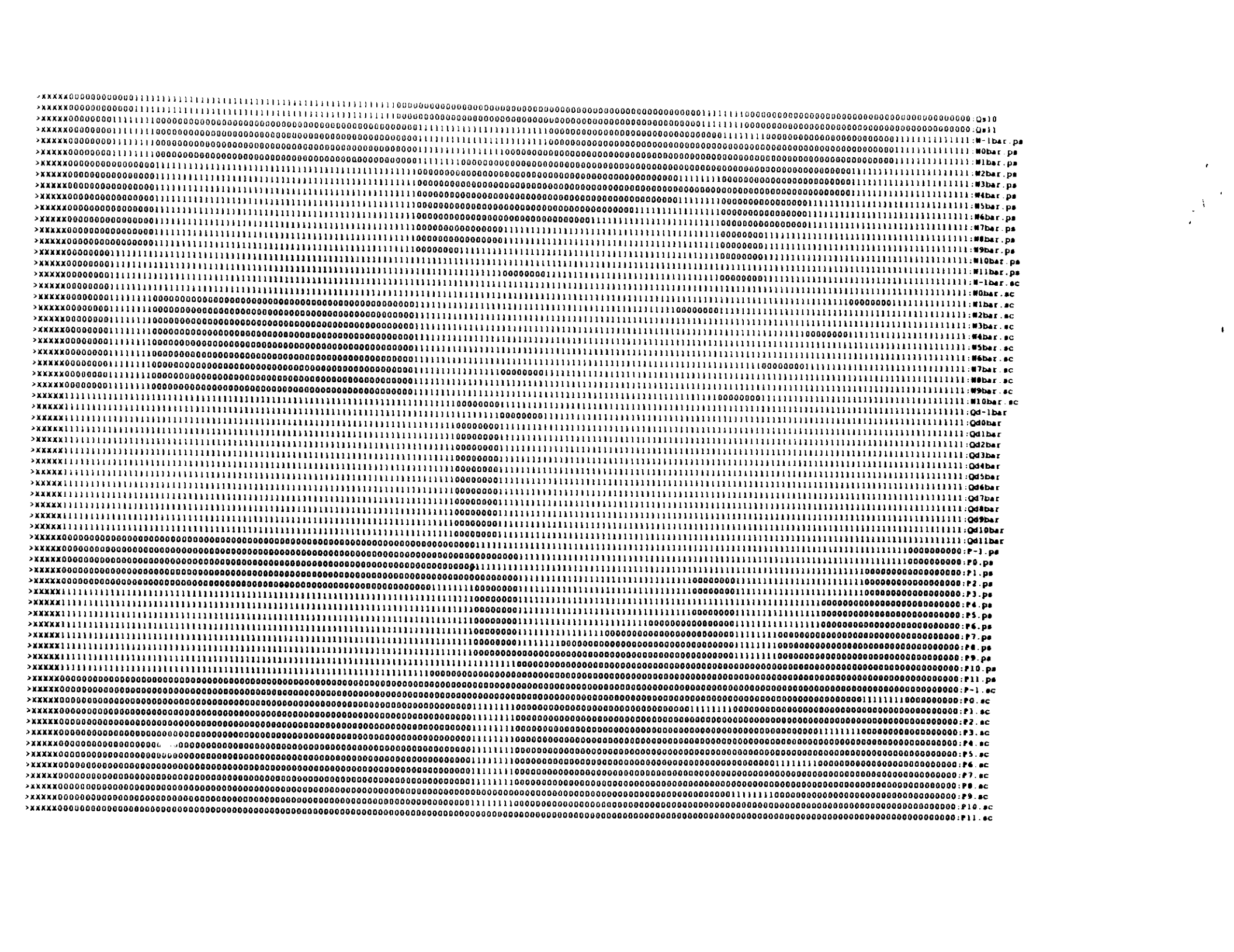
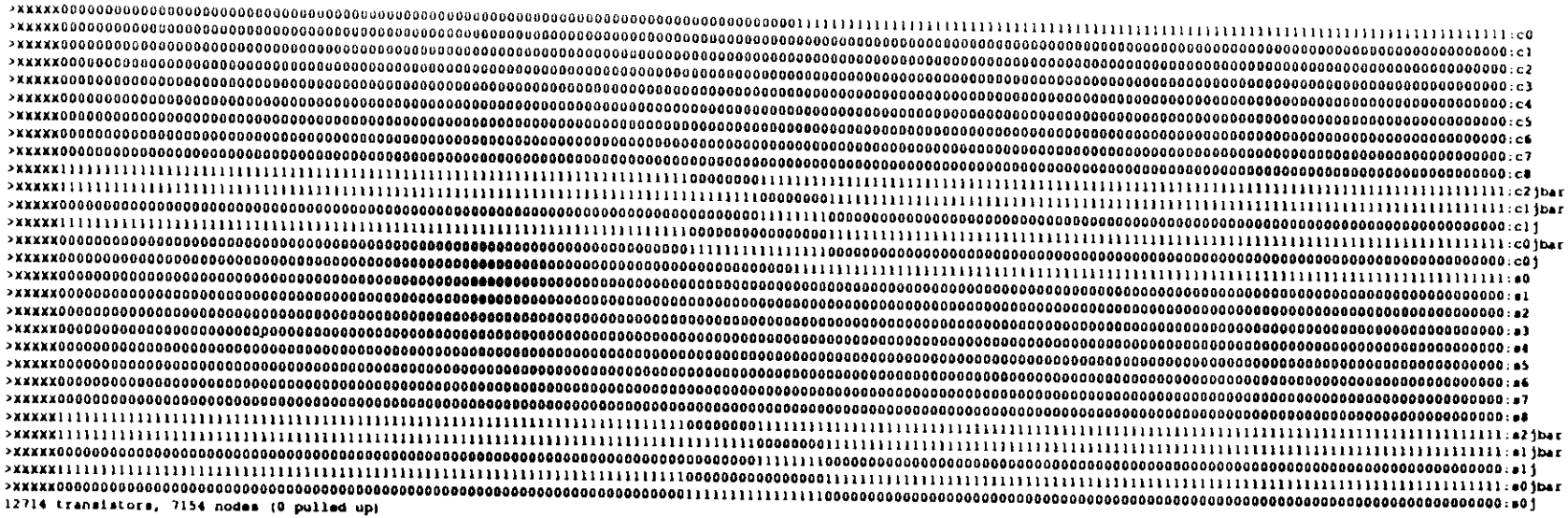
Qd0
Qd1
Qd2
Qd3






12714 transistors, 7154 nodes (0 pulled up)

maui:faris

case5.out

Thu Dec 15 00:15:33 1988

pub3 / Public 3

pub3 maui:faris Job: case5.out Date: Thu Dec 15 00:15:33 1988

pub3 maui:faris Job: case5.out Date: Thu Dec 15 00:15:33 1988

pub3 maui:faris Job: case5.out Date: Thu Dec 15 00:15:33 1988

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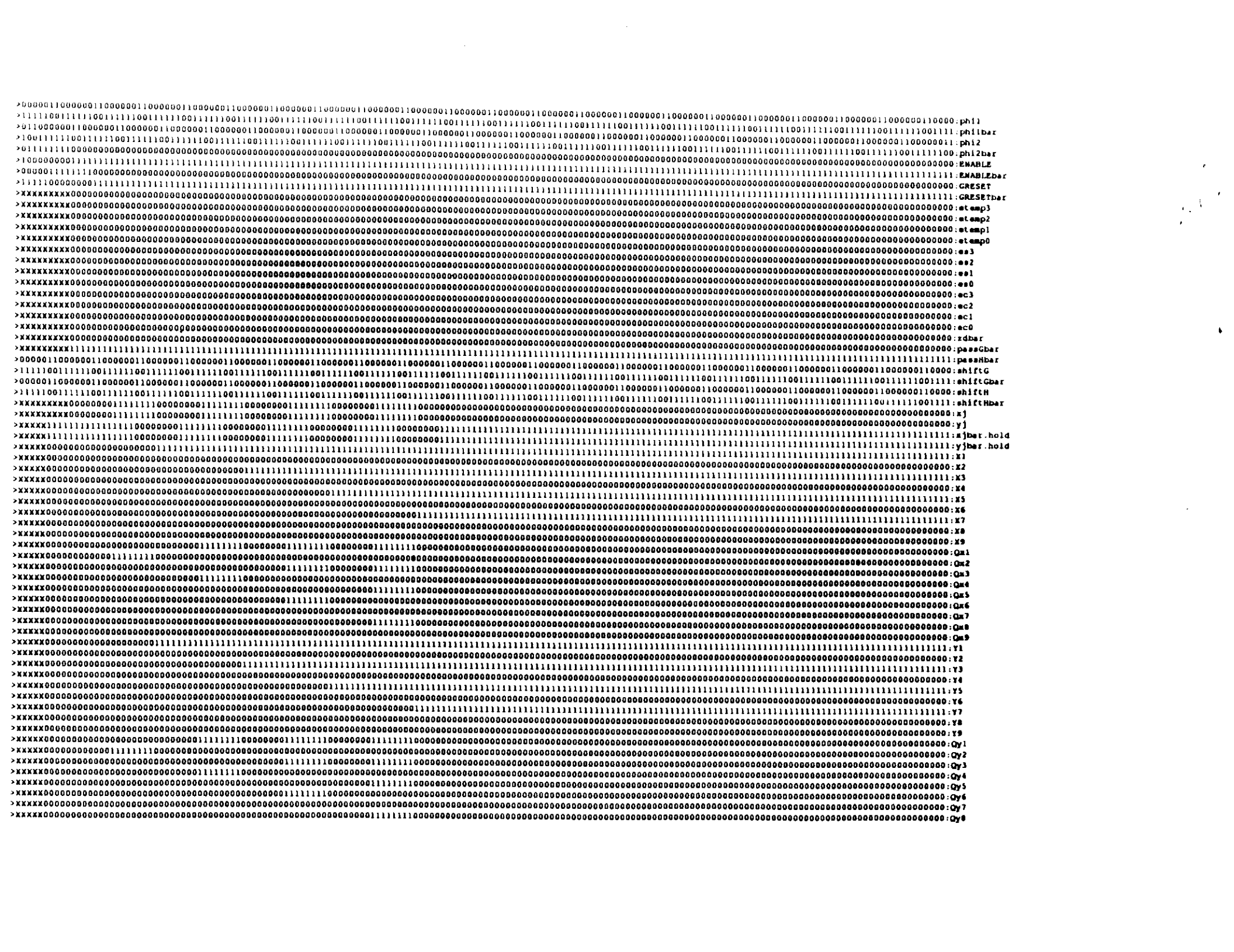
phi1
phi1bar
phi2
phi2bar
ENABLE
ENABLEbar
GRESET
GRESETbar
etemp3
etemp2
etemp1
etemp0
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es2
es1
es0
ec3
ec2
ec1
ec0
xdbar
passGbar
passHbar
shiftG
shiftGbar
shiftH
shiftHbar
xj
yj
xjbar.hold
yjbar.hold
X1
X2
X3
X4
X5
X6
X7
X8
X9
Qx1
Qx2
Qx3
Qx4
Qx5
Qx6
Qx7
Qx8
Qx9
Y1
Y2
Y3
Y4
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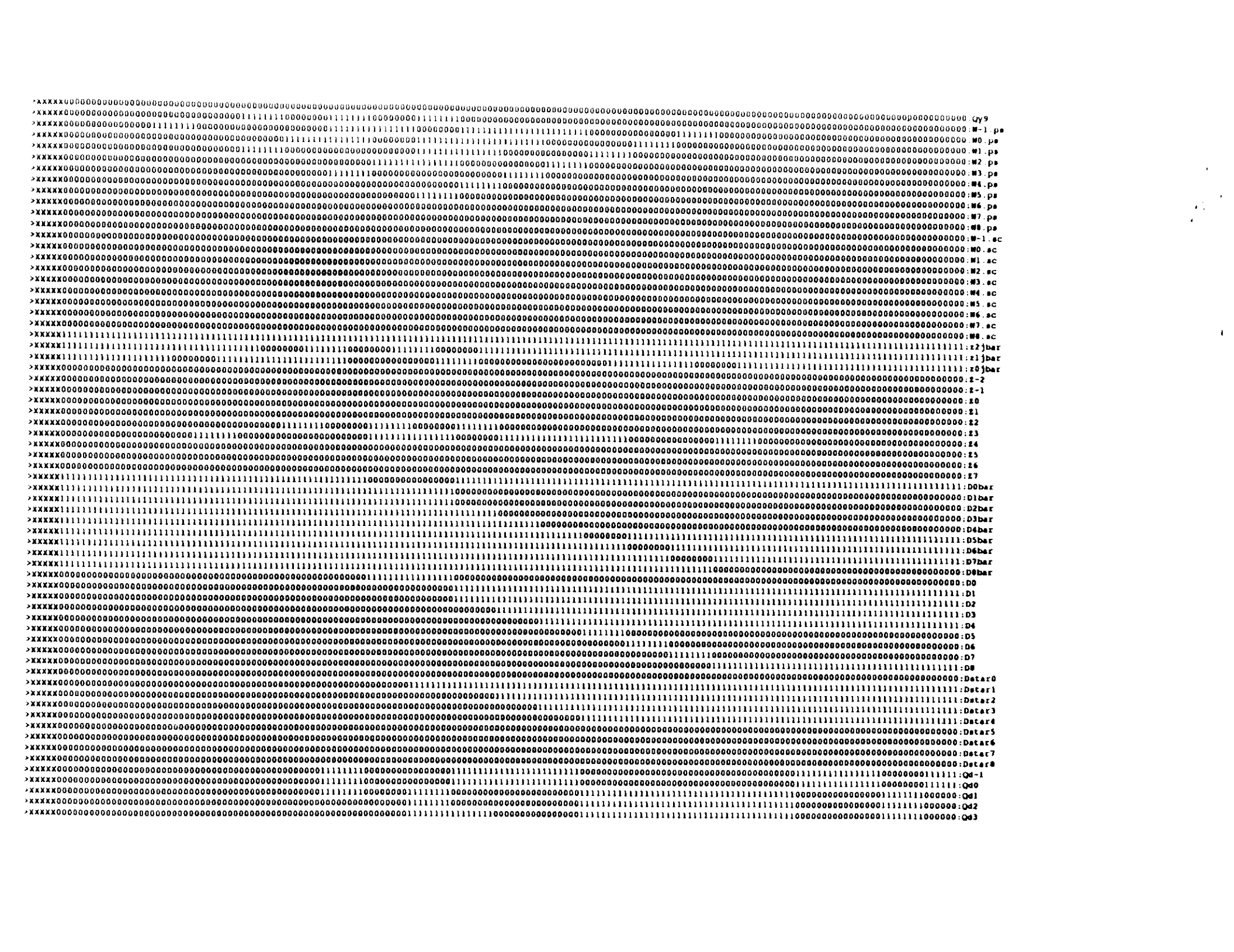
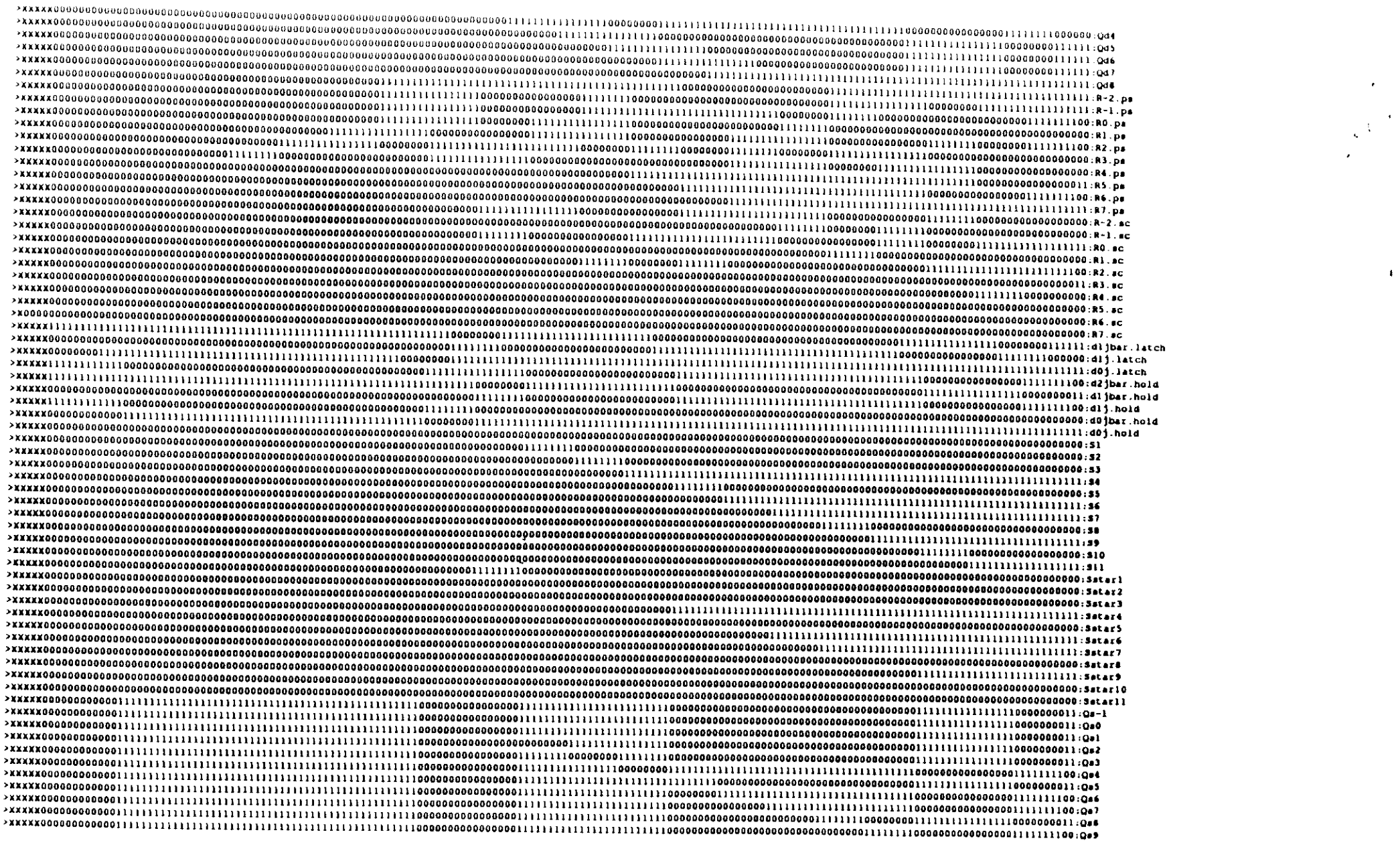
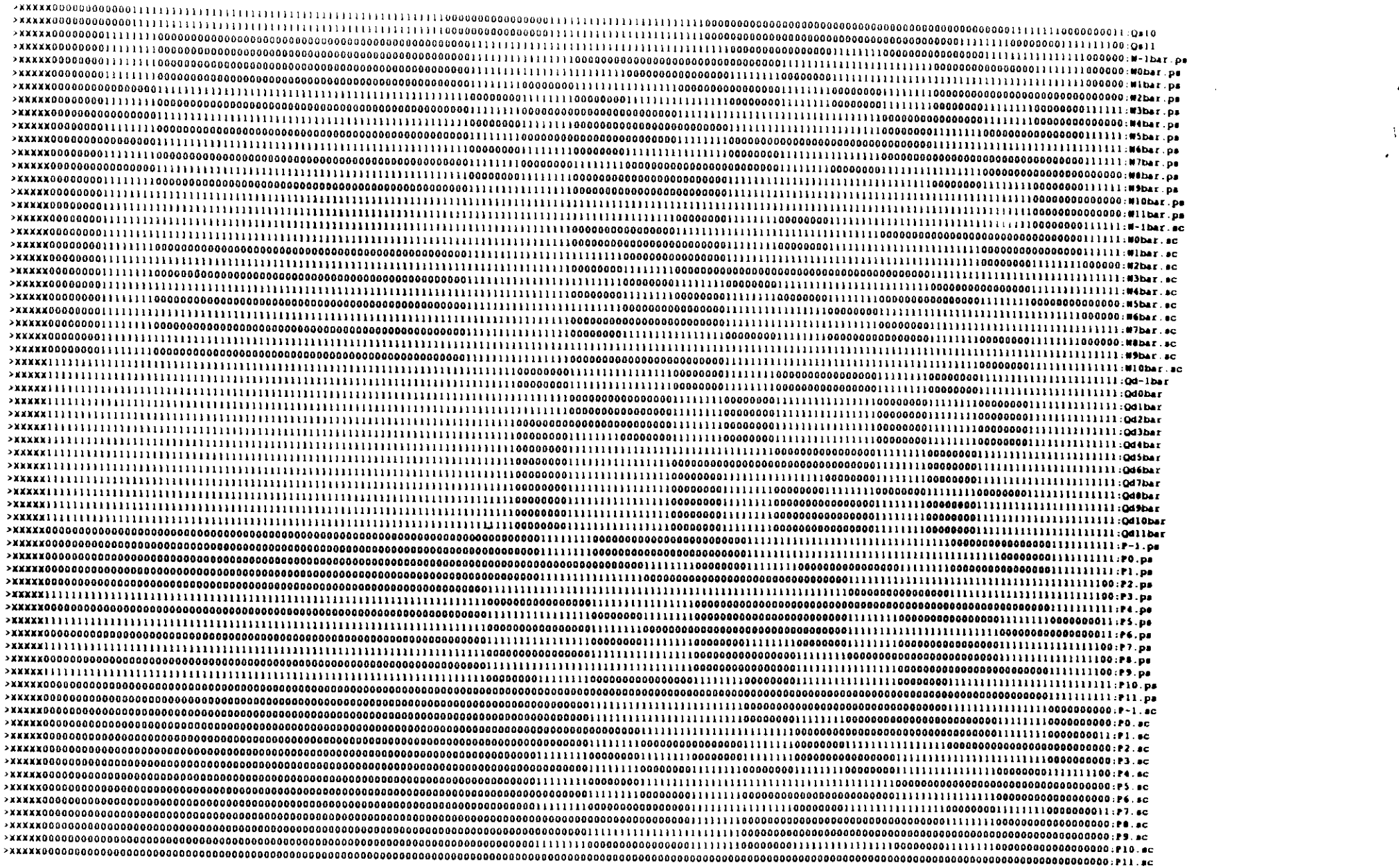
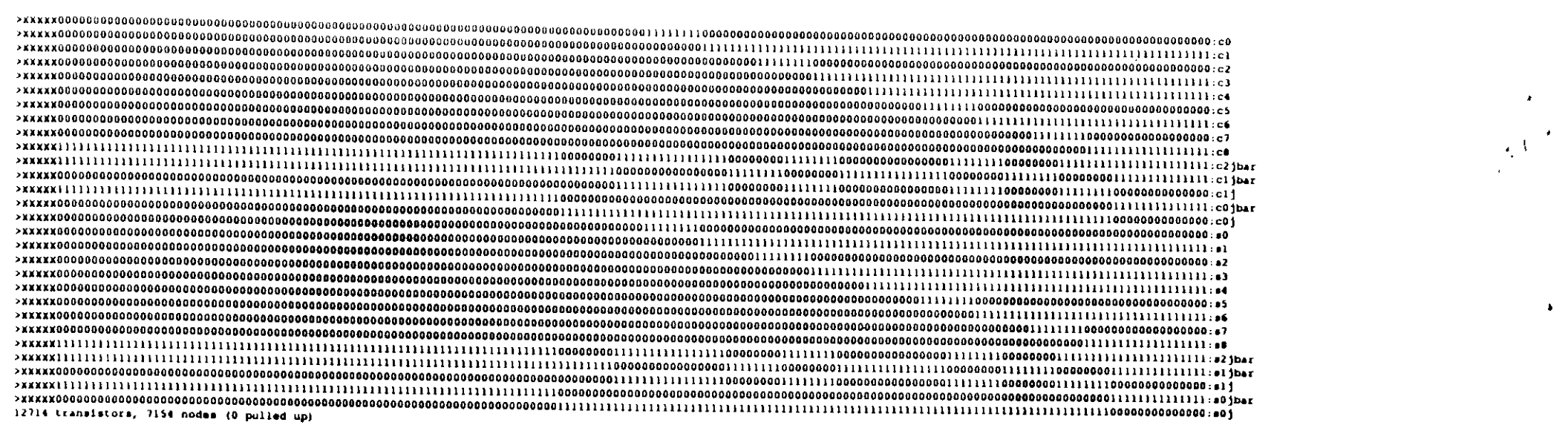
Qy3
Qy4
Qy5
Qy6
Qy7
Qy8









12714 transistors, 7154 nodes (0 pulled up)

maui:faris

case6.out

Thu Dec 15 00:17:55 1988

pub3 / Public 3

pub3 maui:faris Job: case6.out Date: Thu Dec 15 00:17:55 1988

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pub3 maui:faris Job: case6.out Date: Thu Dec 15 00:17:55 1988

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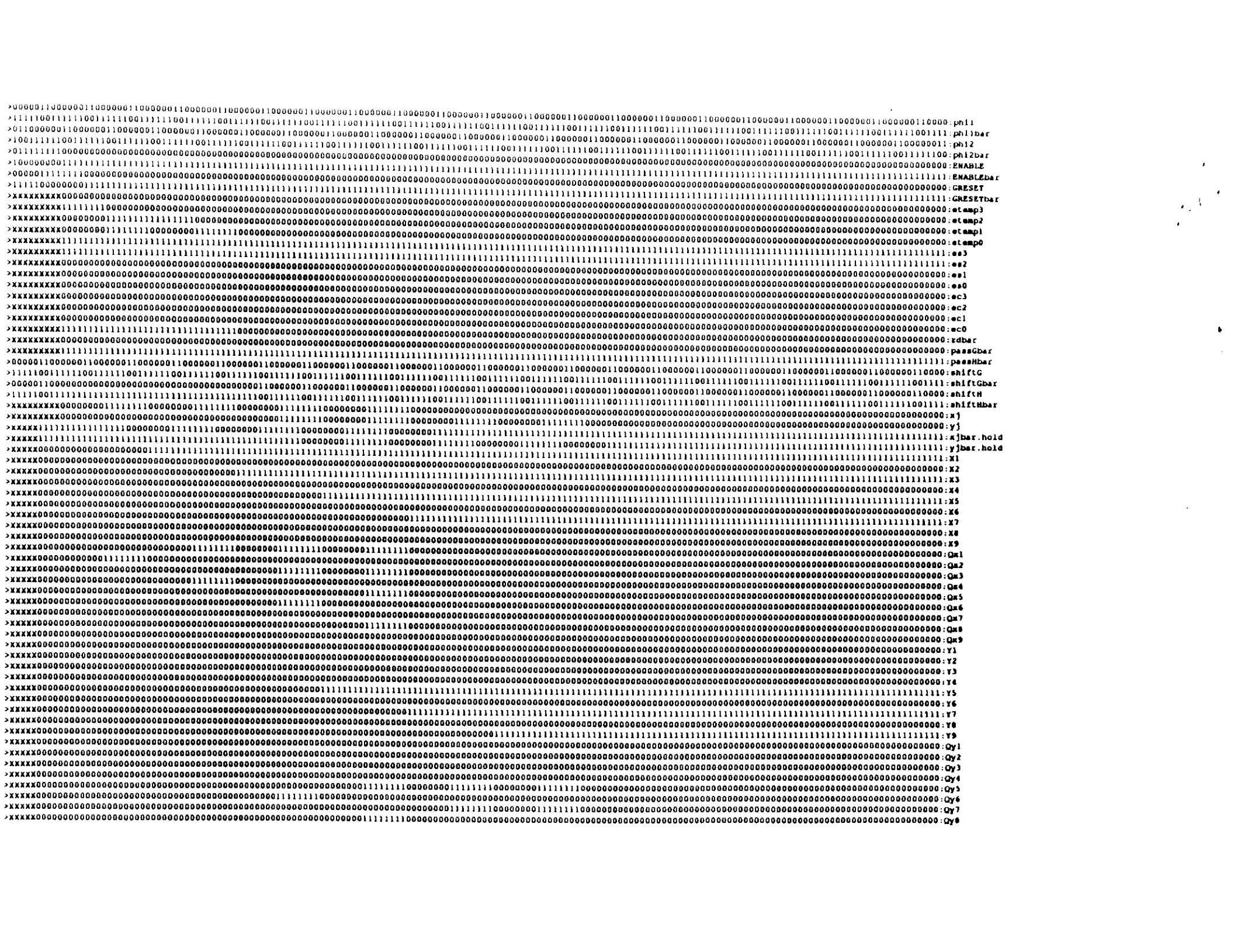

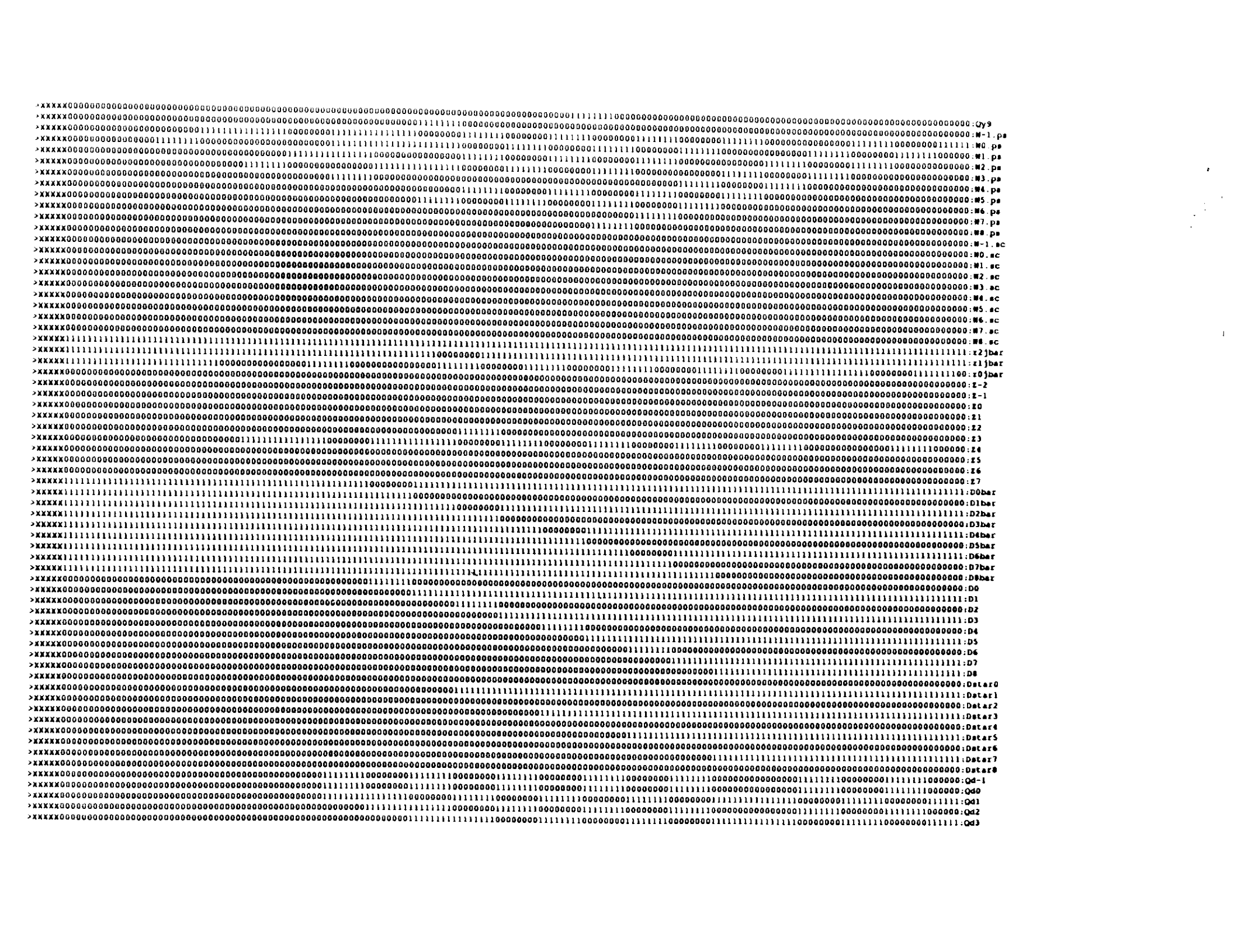

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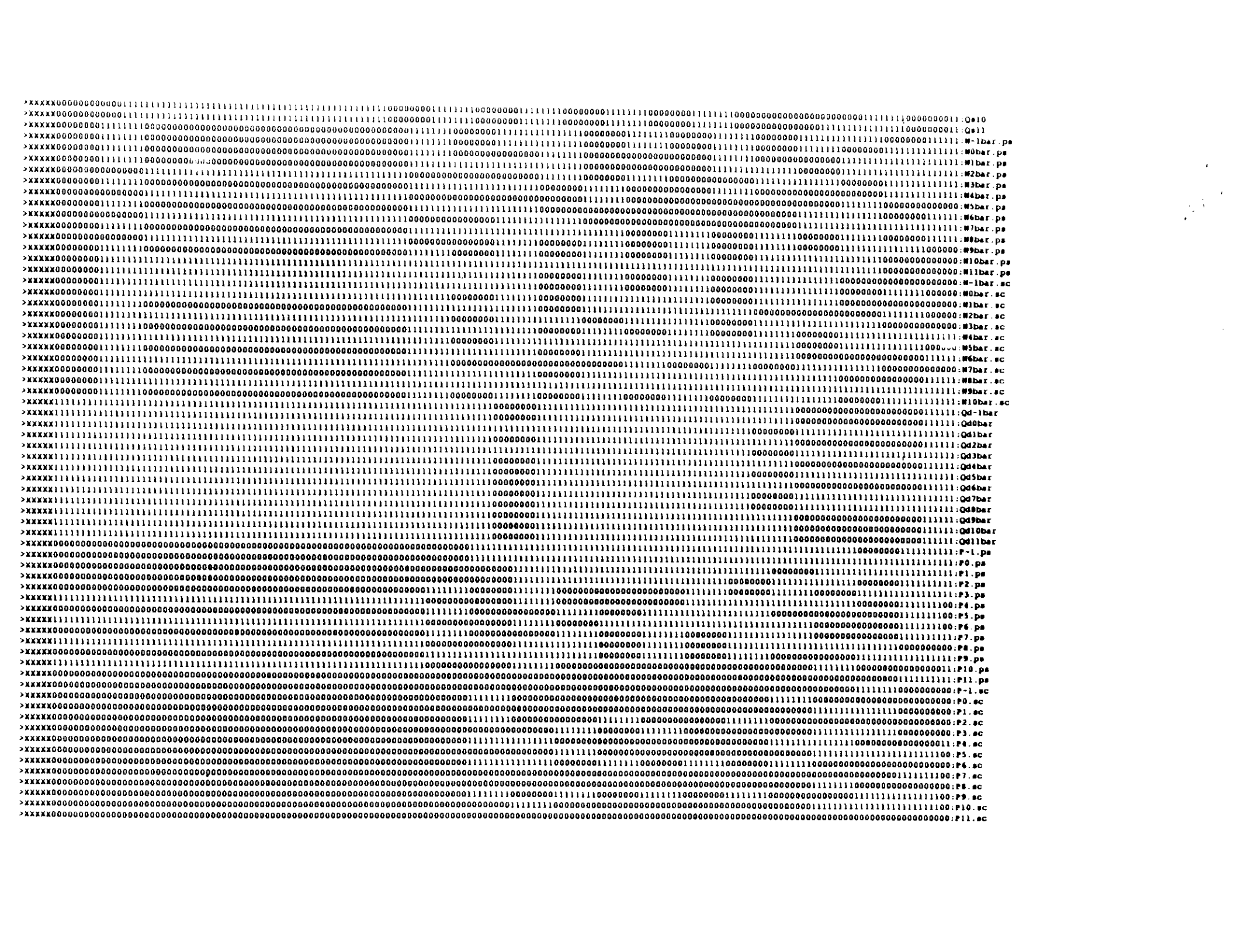

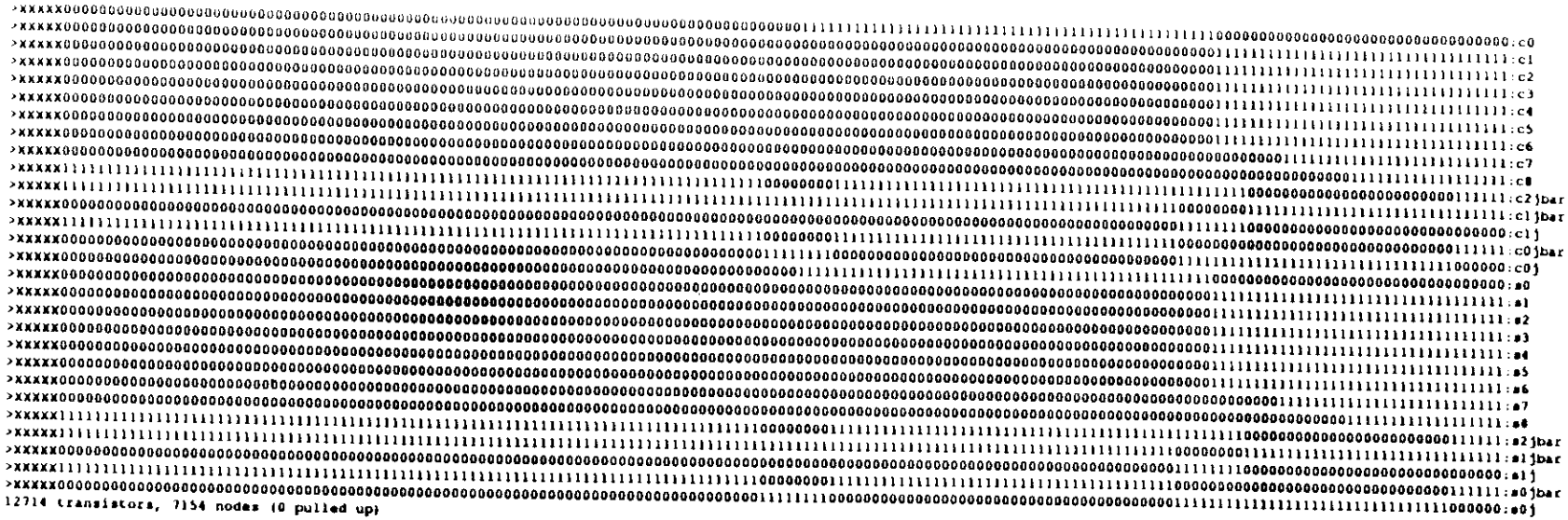

12714 transistors, 7154 nodes (0 pulled up)

[redacted]

maui:faris

case7.out

Thu Dec 15 00:20:18 1988

pub3 / Public 3

[redacted]

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pub3 maui:faris  Job: case7.out  Date: Thu Dec 15 00:20:18 1988

pub3 maui:faris  Job: case7.out  Date: Thu Dec 15 00:20:18 1988

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pub3 maui:faris  Job: case7.out  Date: Thu Dec 15 00:20:18 1988
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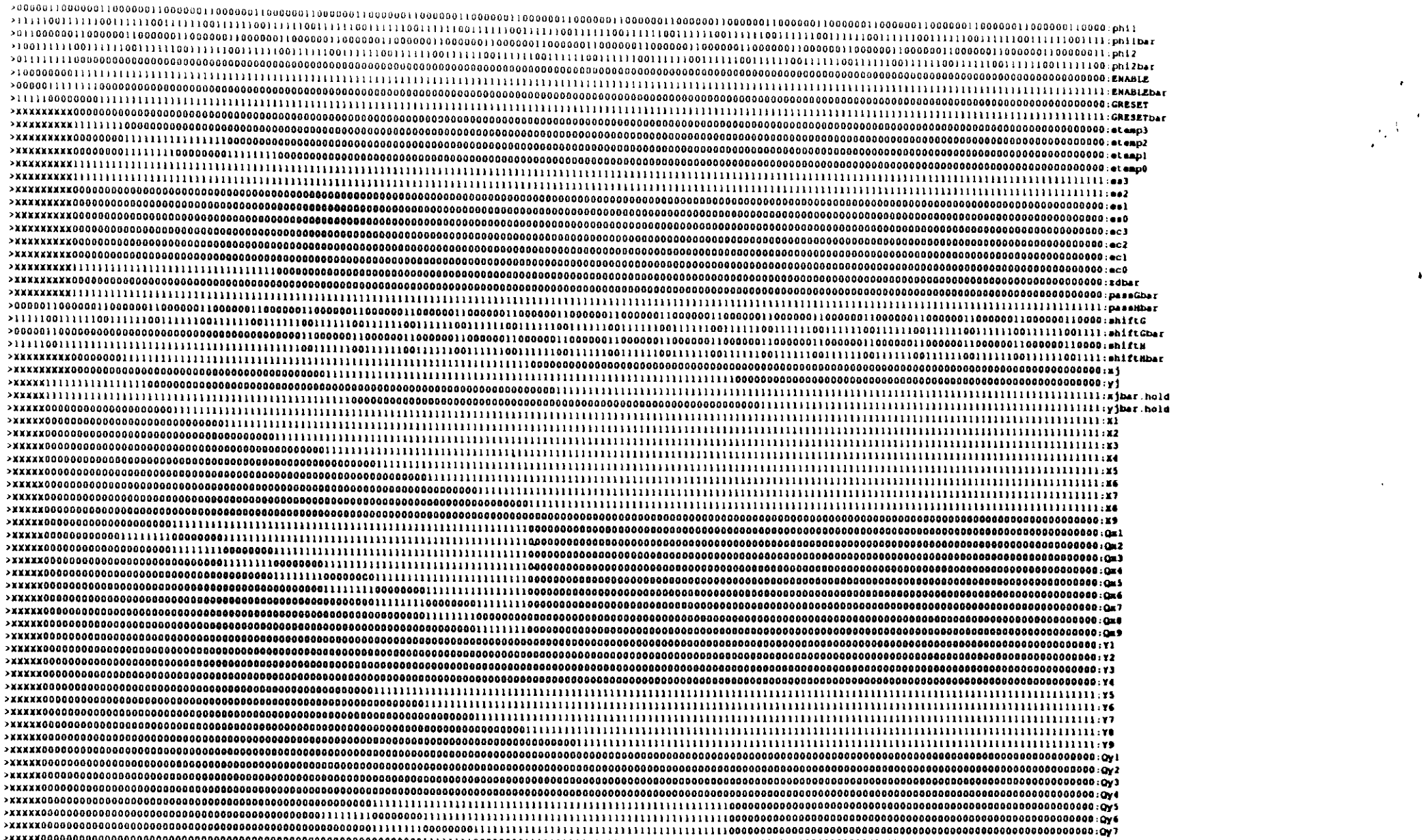
phi1
phi1bar
phi2
phi2bar
ENABLE
ENABLEbar
GRESET
GRESETbar
etemp3
etemp2
etemp1
etemp0
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es2
es1
es0
ec3
ec2
ec1
ec0
zdbar
passGbar
passMbar
shiftG
shiftGbar
shiftM
shiftMbar
xj
yj
xjbar.hold
yjbar.hold
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X2
X3
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X7
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Y3
Y4
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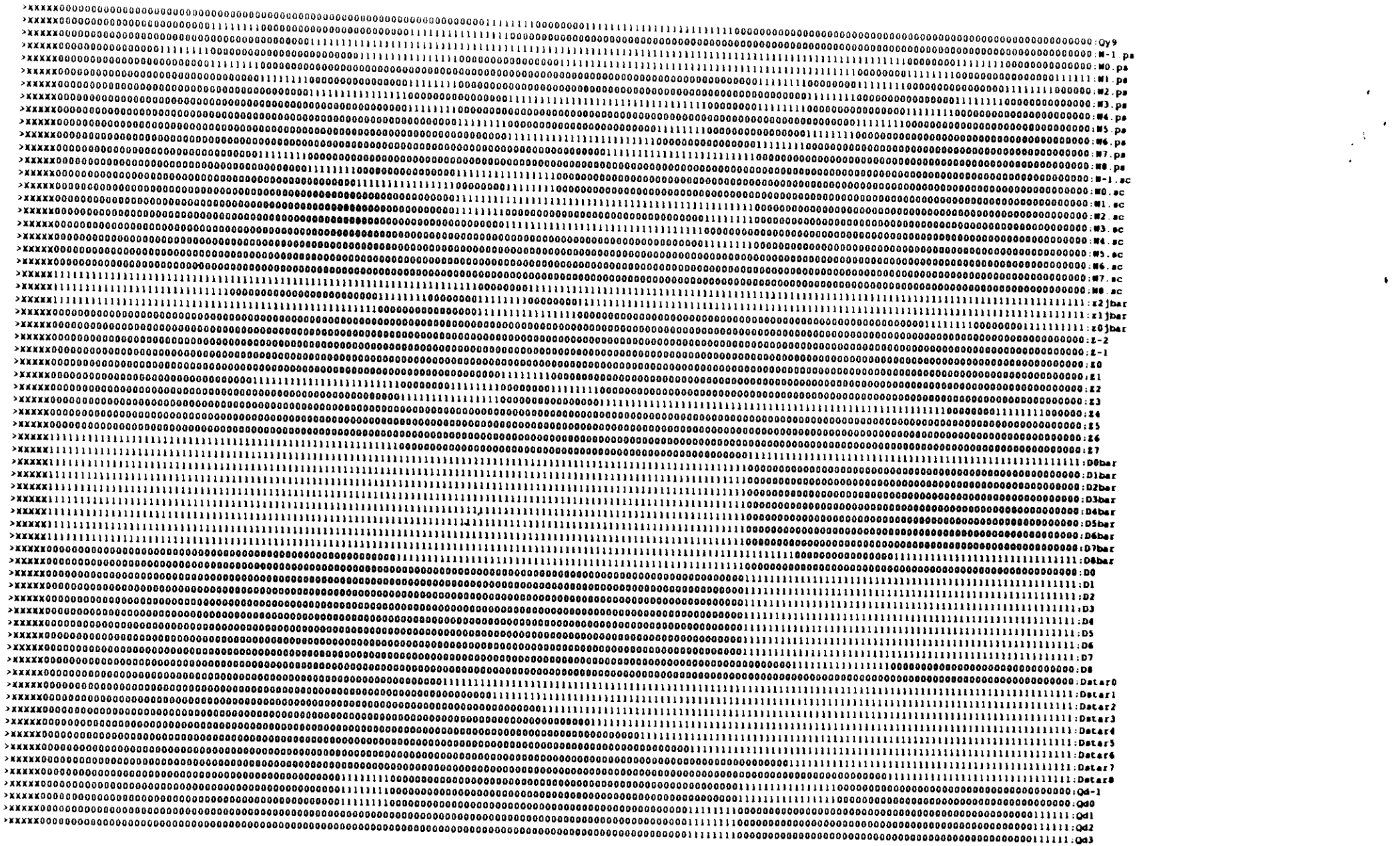
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M0.ps
M1.ps
M2.ps
M3.ps
M4.ps
M5.ps
M6.ps
M7.ps
M8.ps
M-1.sc
M0.sc
M1.sc
M2.sc
M3.sc
M4.sc
M5.sc
M6.sc
M7.sc
M8.sc
x2jbar
x1jbar
x0jbar
Z-2
Z-1
Z0
Z1
Z2
Z3
Z4
Z5
Z6
Z7
D0bar
D1bar
D2bar
D3bar
D4bar
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D3
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D7
D8
Dstar0
Dstar1
Dstar2
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Dstar7
Dstar8
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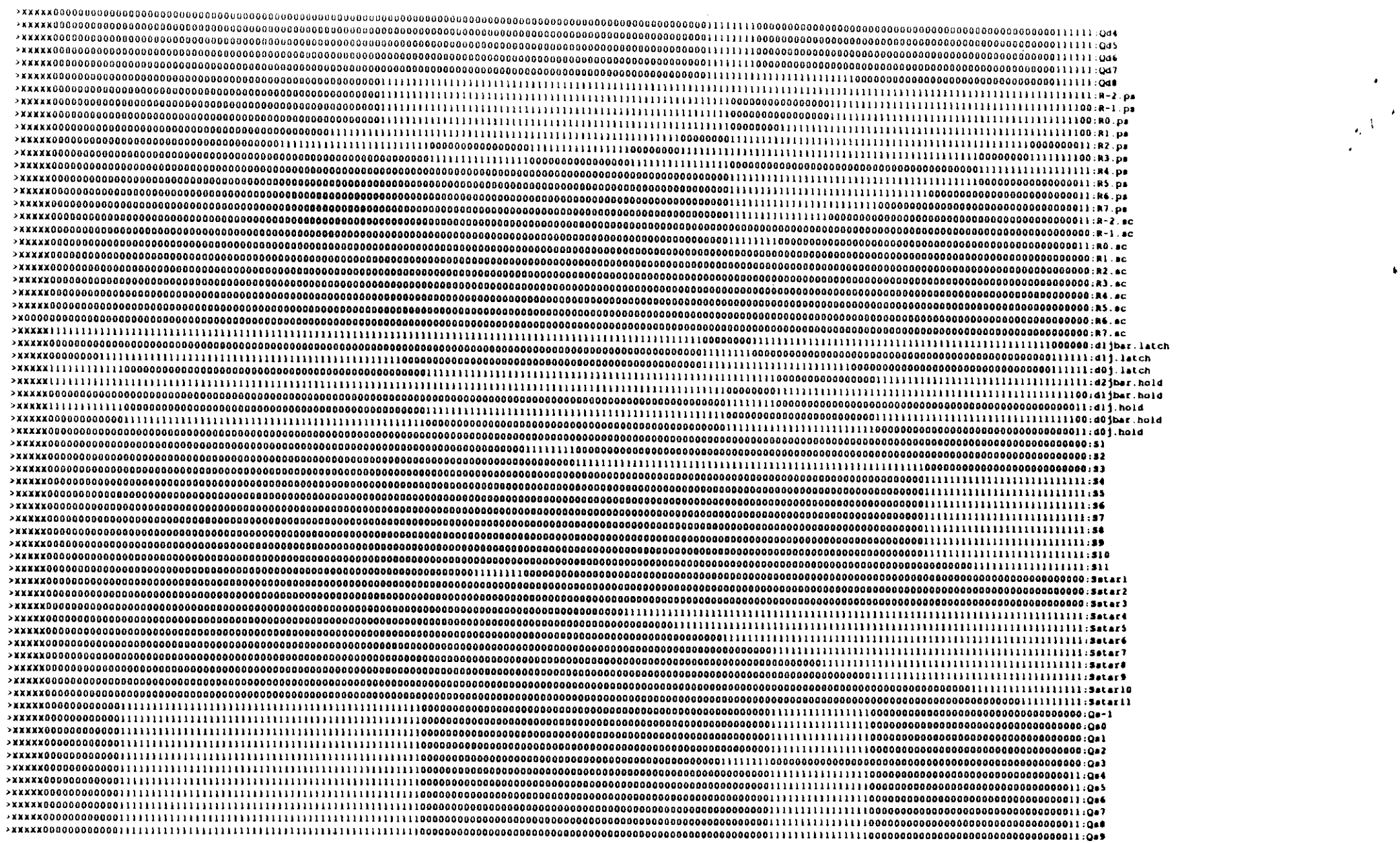
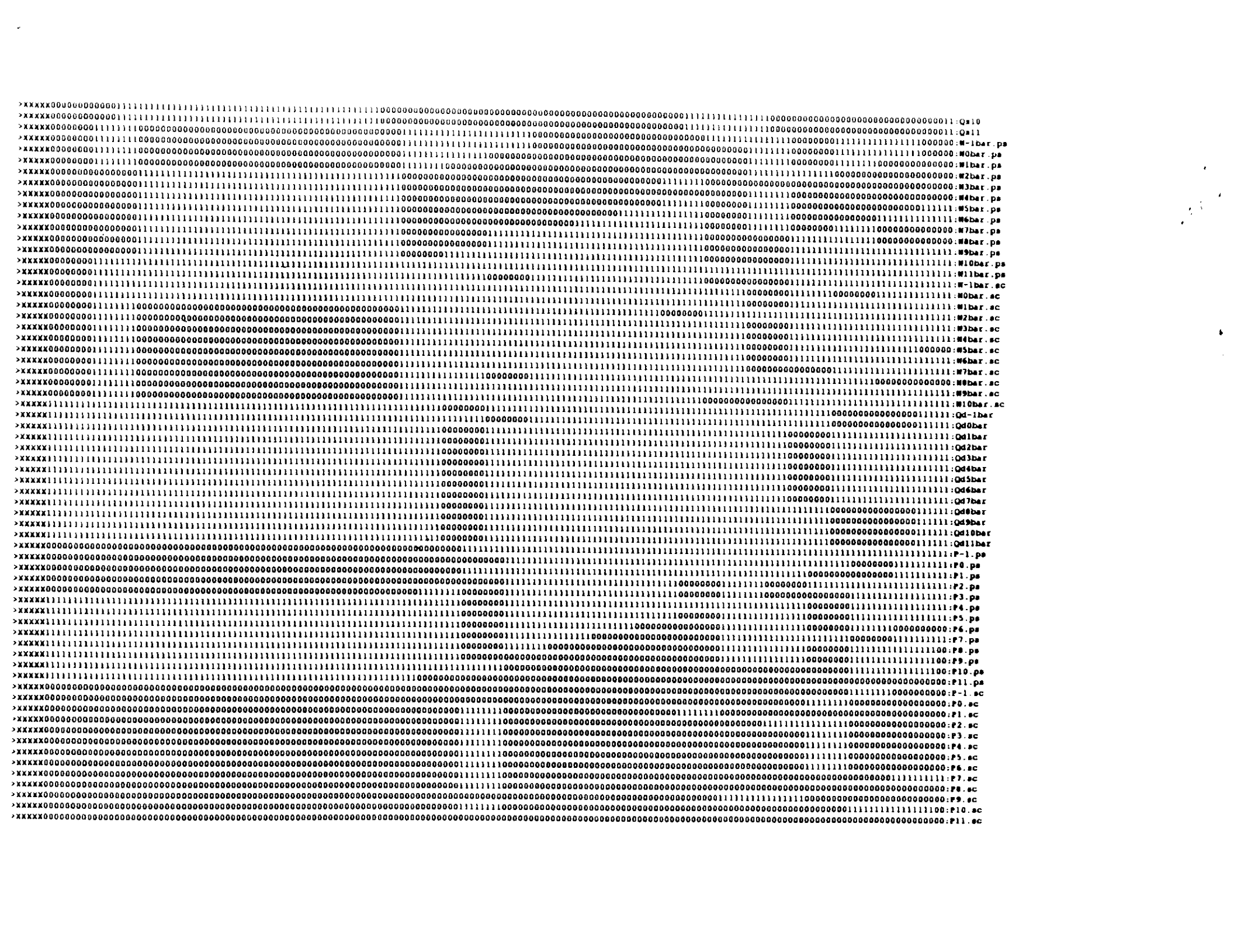
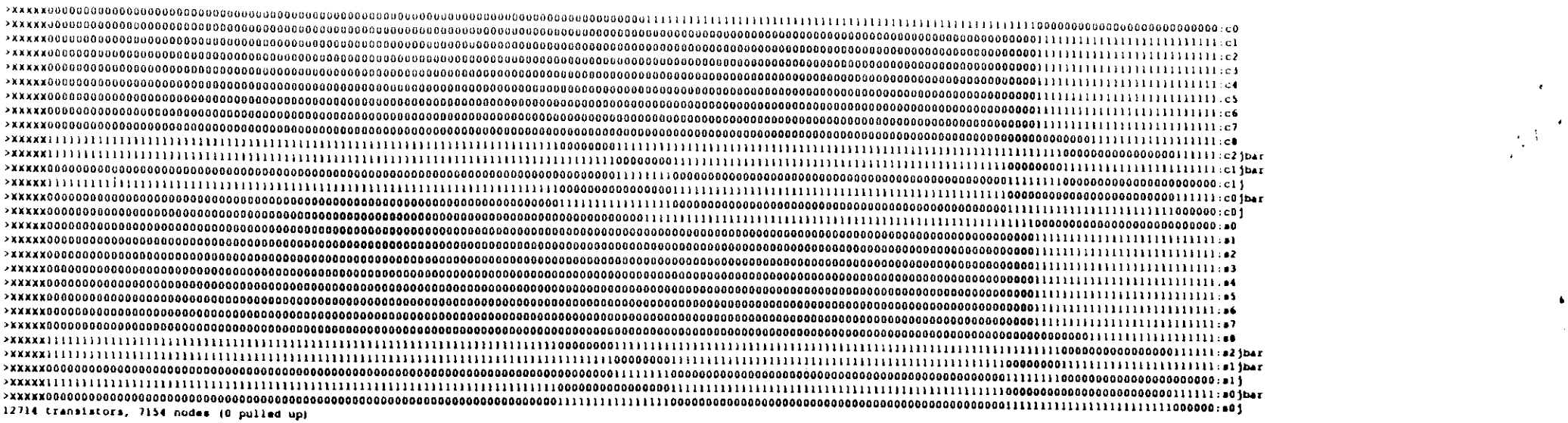
Qd1
Qd2
Qd3


Qd4
Qd5
Qd6
Qd7
Qd8
R-2.ps
R-1.ps
R0.ps
R1.ps
R2.ps
R3.ps
R4.ps
R5.ps
R6.ps
R7.ps
R-2.sc
R-1.sc
R0.sc
R1.sc
R2.sc
R3.sc
R4.sc
R5.sc
R6.sc
R7.sc
d1jbar.latch
d1j.latch
d0j.latch
d2jbar.hold
d1jbar.hold
d1j.hold
d0jbar.hold
d0j.hold
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
Sstar1
Sstar2
Sstar3
Sstar4
Sstar5
Sstar6
Sstar7
Sstar8
Sstar9
Sstar10
Sstar11
Qs-1
Qs0
Qs1
Qs2
Qs3
Qs4
Qs5
Qs6
Qs7
Qs8
Qs9





12714 transistors, 7154 nodes (0 pulled up)

maui:faris

case8.out

Thu Dec 15 00:22:40 1988

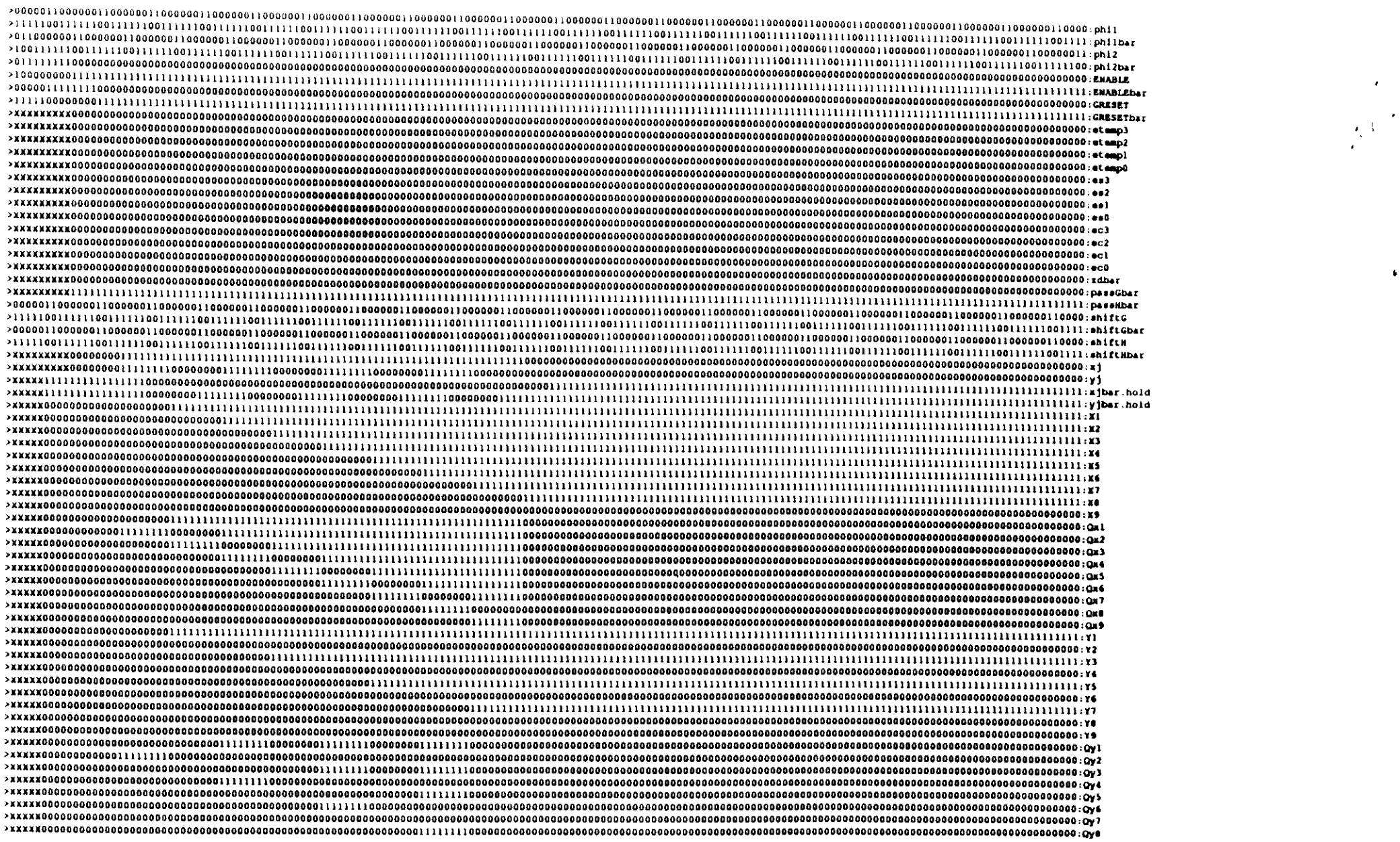
pub3 / Public 3

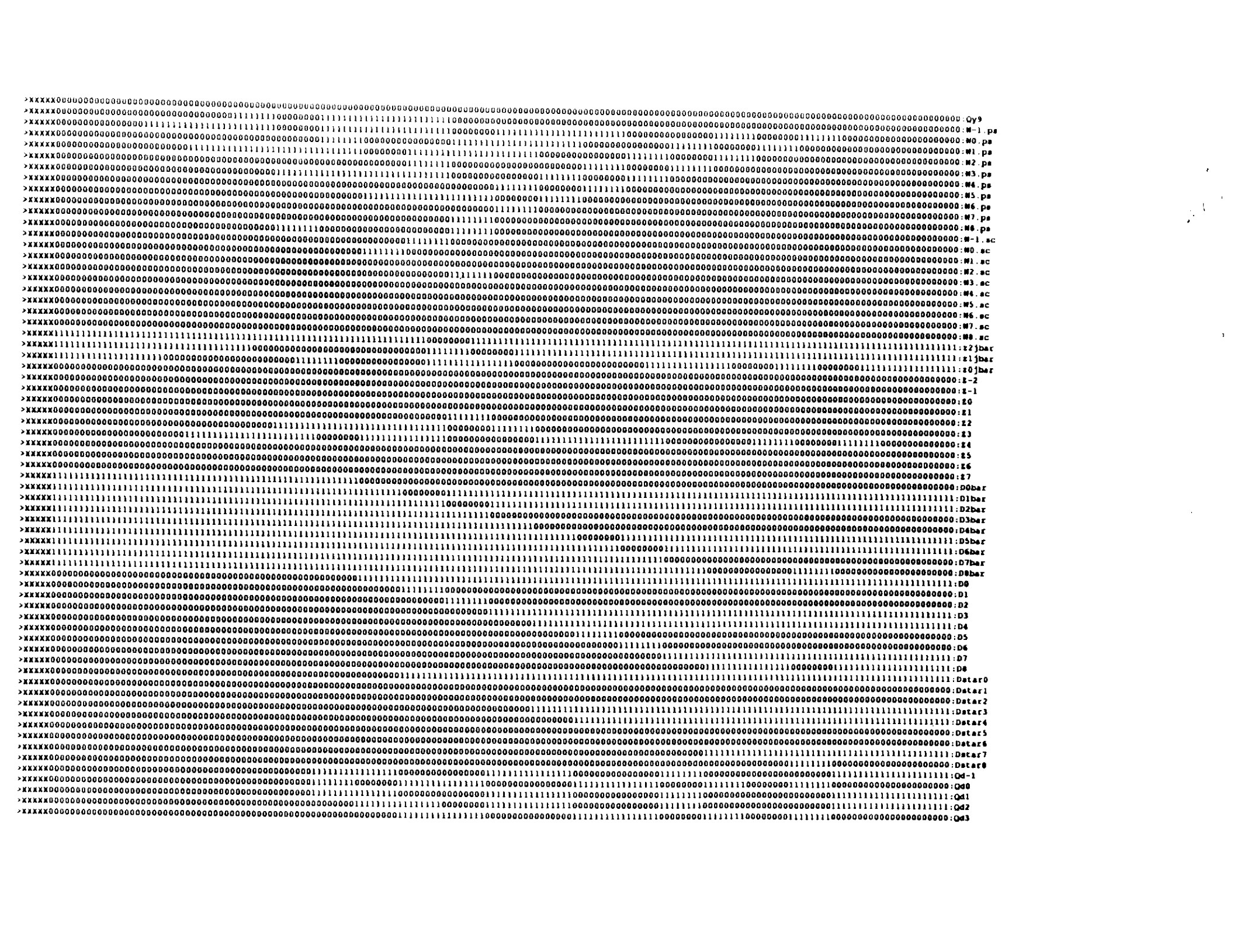
pub3 maui:faris Job: case8.out Date: Thu Dec 15 00:22:40 1988

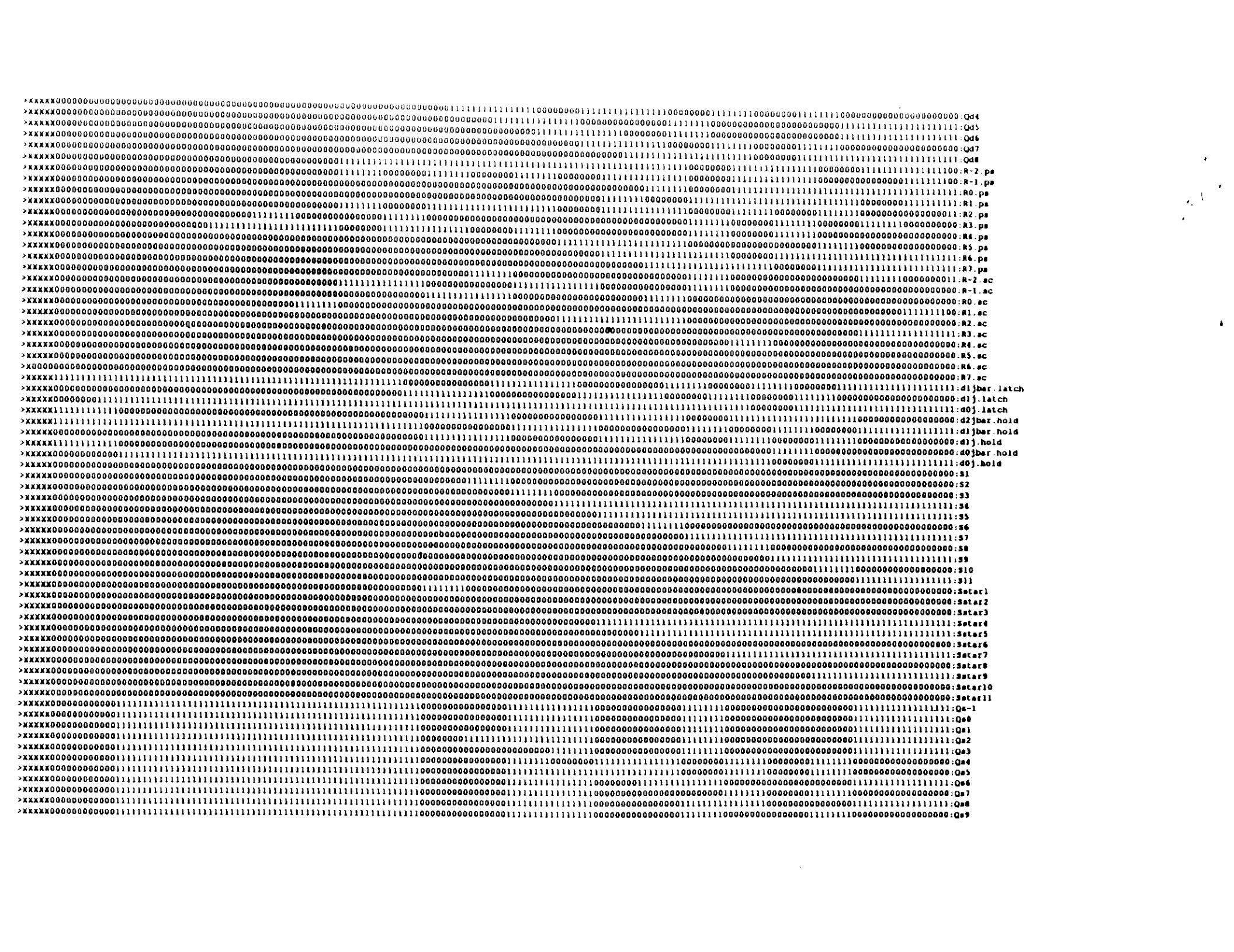
pub3 maui:faris Job: case8.out Date: Thu Dec 15 00:22:40 1988

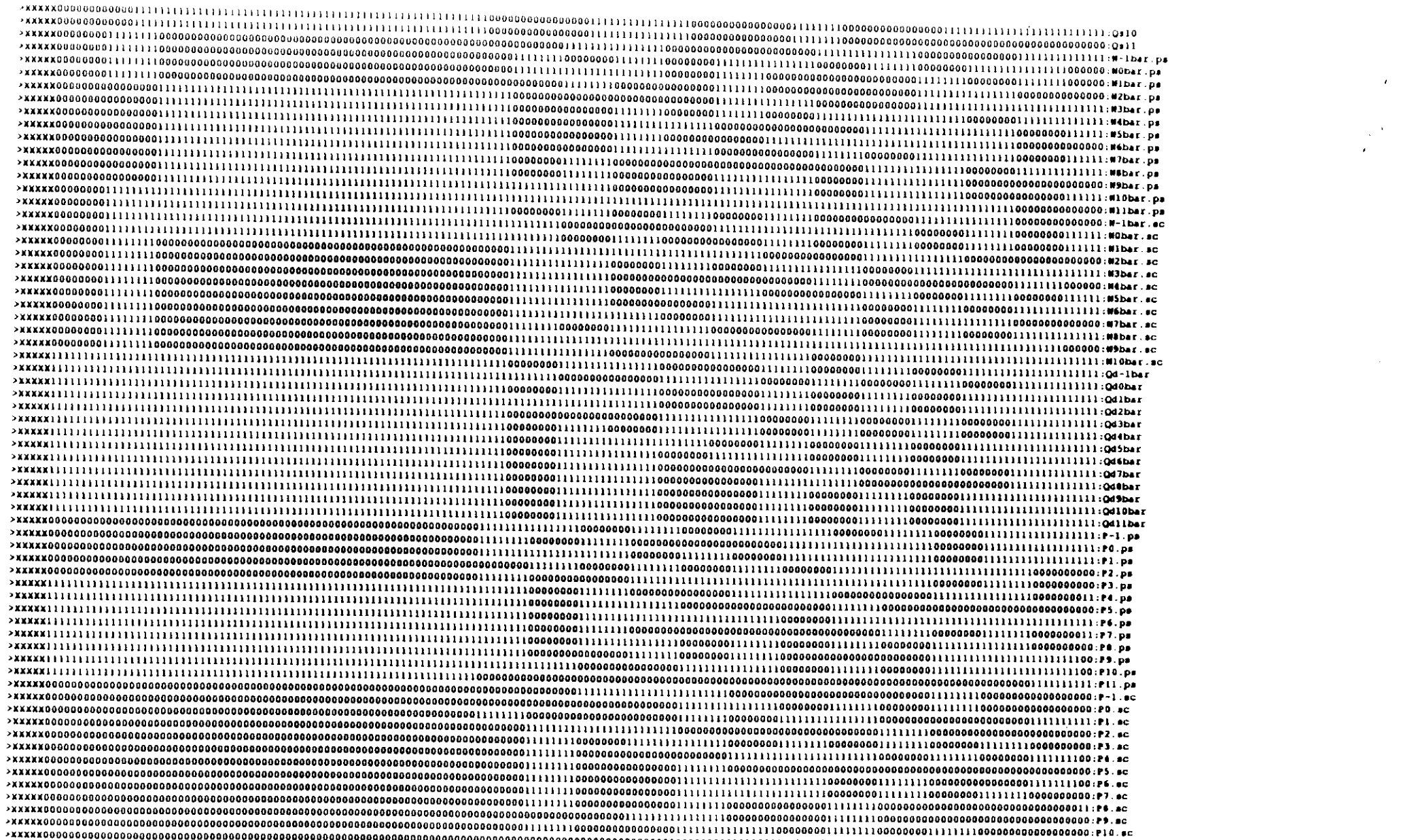
pub3 maui:faris Job: case8.out Date: Thu Dec 15 00:22:40 1988

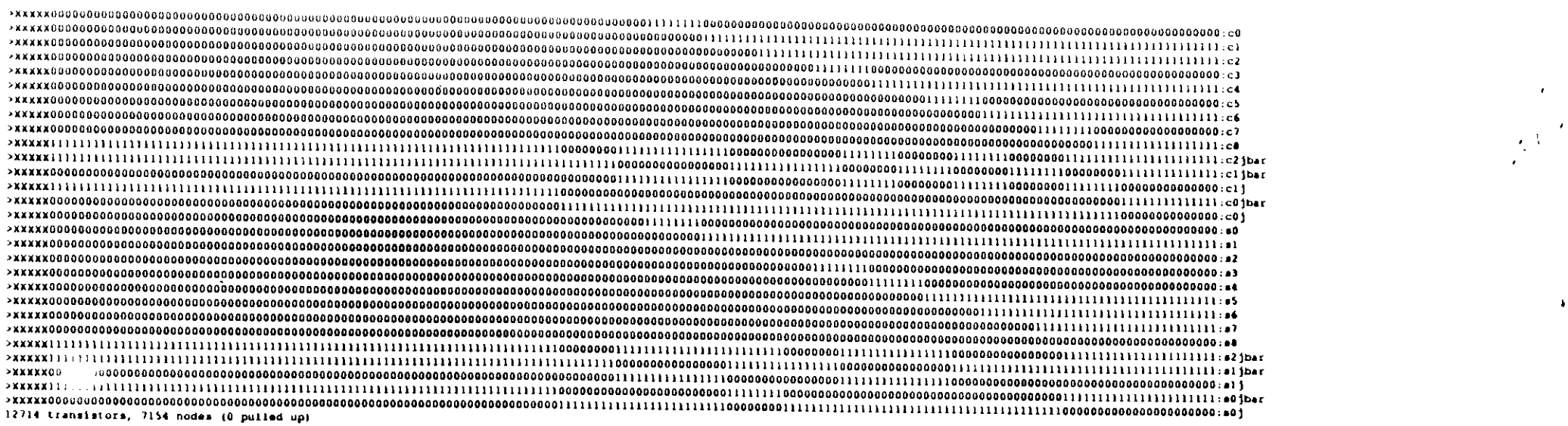
pub3 maui:faris Job: case8.out Date: Thu Dec 15 00:22:40 1988


phi1
phi1bar
phi2
phi2bar
ENABLE
ENABLEbar
GRESET
GRESETbar
etemp3
etemp2
etemp1
etemp0
es3
es2
es1
es0
ec3
ec2
ec1
ec0
xdbar
passGbar
passHbar
shiftG
shiftGbar
shiftH
shiftHbar
xj
yj
xjbar.hold
yjbar.hold
X1
X2
X3
X4
X5
X6
X7
X8
X9
Qx1
Qx2
Qx3
Qx4
Qx5
Qx6
Qx7
Qx8
Qx9
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
Qy1
Qy2
Qy3
Qy4
Qy5
Qy6
Qy7
Qy8




Qd4
Qd5
Qd6
Qd7
Qd8
R-2.ps
R-1.ps
R0.ps
R1.ps
R2.ps
R3.ps
R4.ps
R5.ps
R6.ps
R7.ps
R-2.sc
R-1.sc
R0.sc
R1.sc
R2.sc
R3.sc
R4.sc
R5.sc
R6.sc
R7.sc
d1jbar.latch
d1j.latch
d0j.latch
d2jbar.hold
d1jbar.hold
d1j.hold
d0jbar.hold
d0j.hold
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
Sstar1
Sstar2
Sstar3
Sstar4
Sstar5
Sstar6
Sstar7
Sstar8
Sstar9
Sstar10
Sstar11
Qs-1
Qs0
Qs1
Qs2
Qs3
Qs4
Qs5
Qs6
Qs7
Qs8
Qs9





12714 transistors, 7154 nodes (0 pulled up)

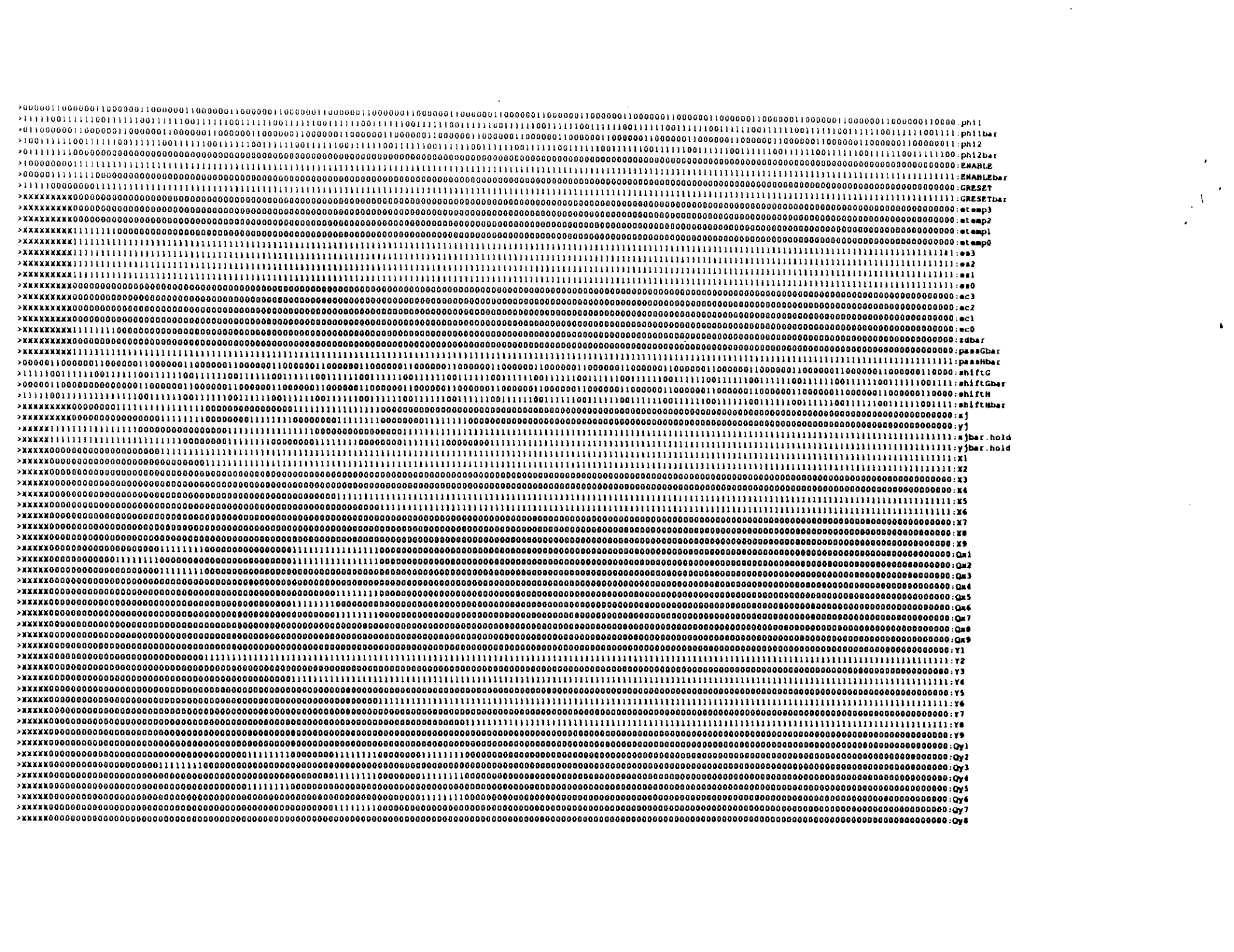
maui:faris

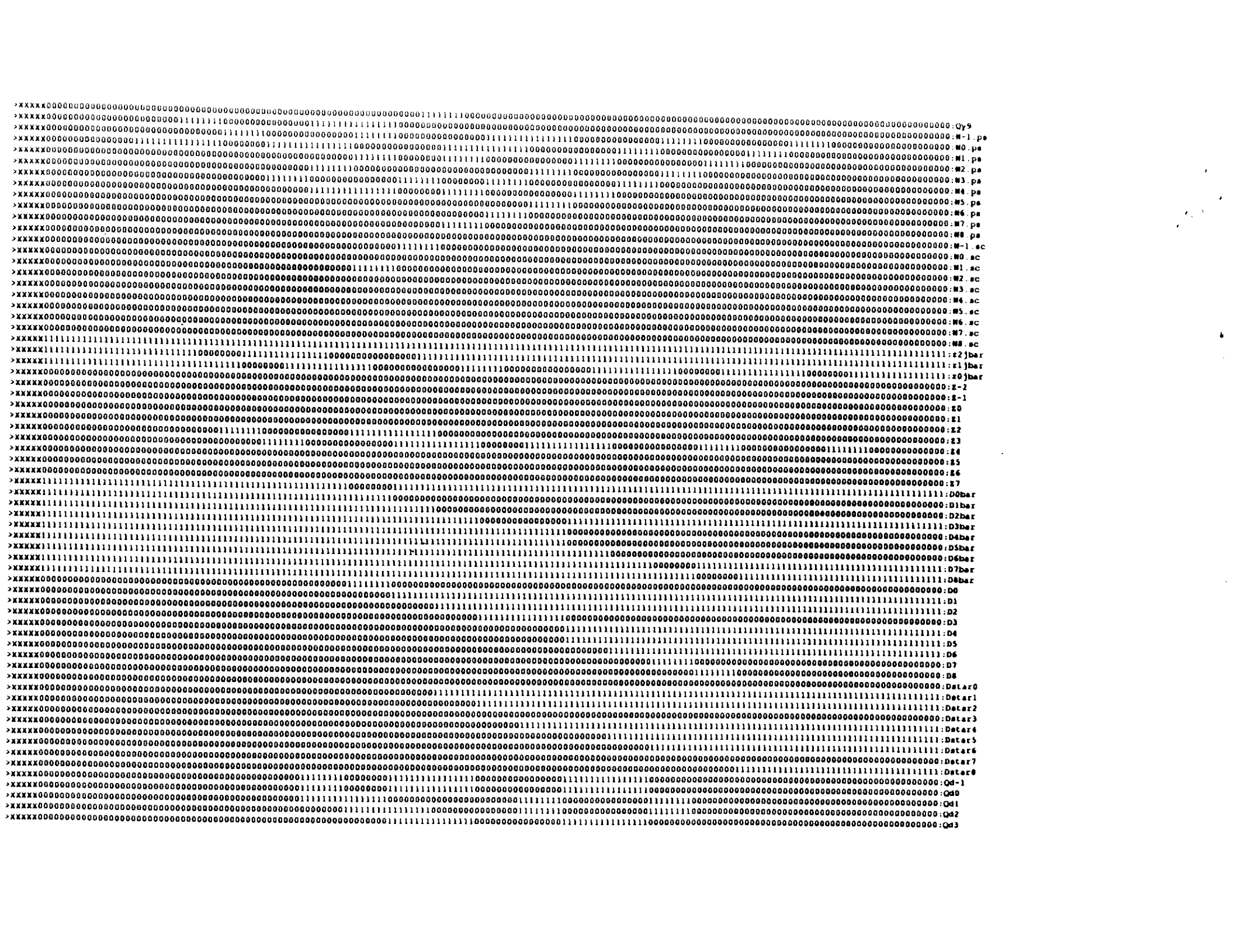
case9.out

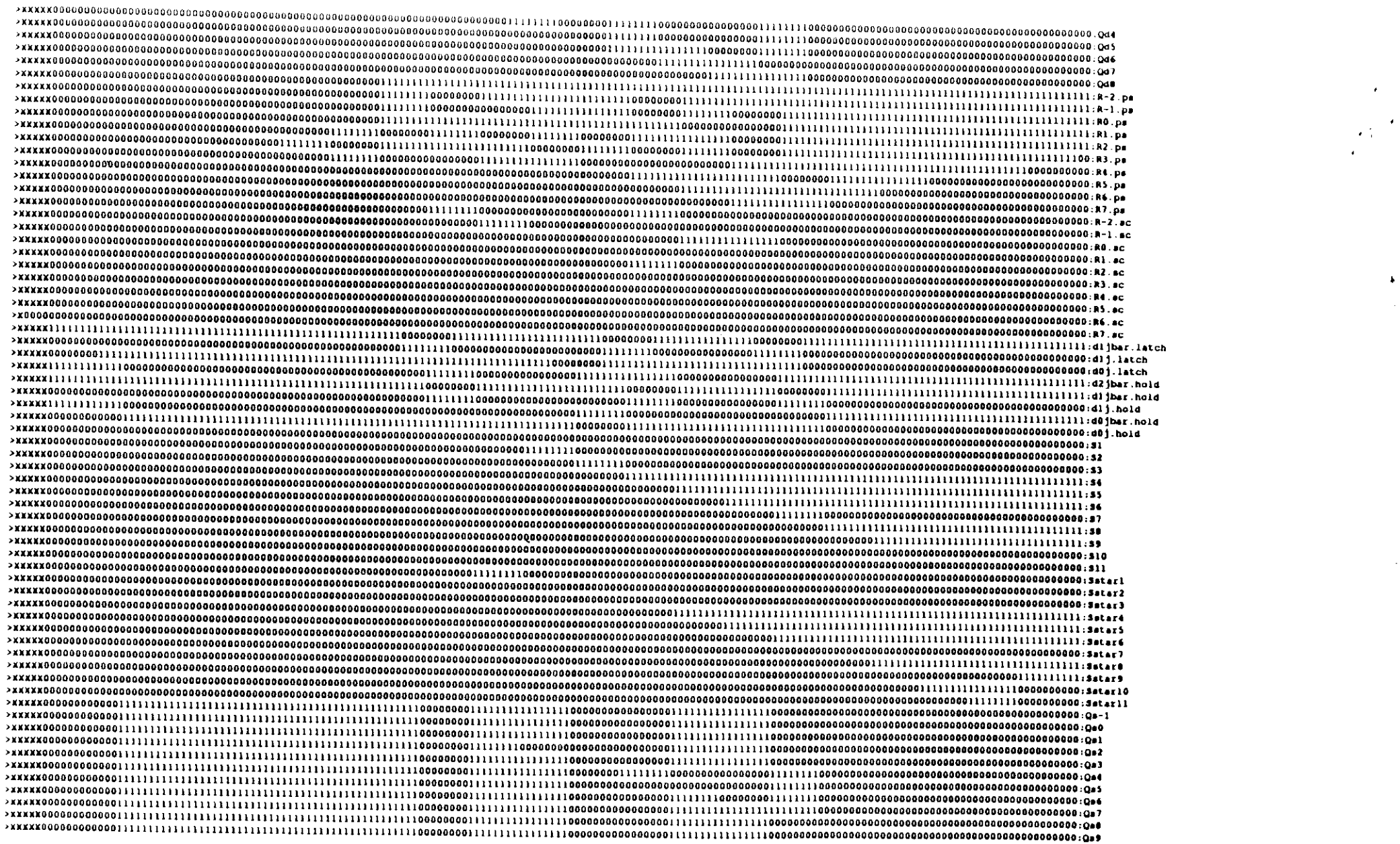
Thu Dec 15 00:25:15 1988

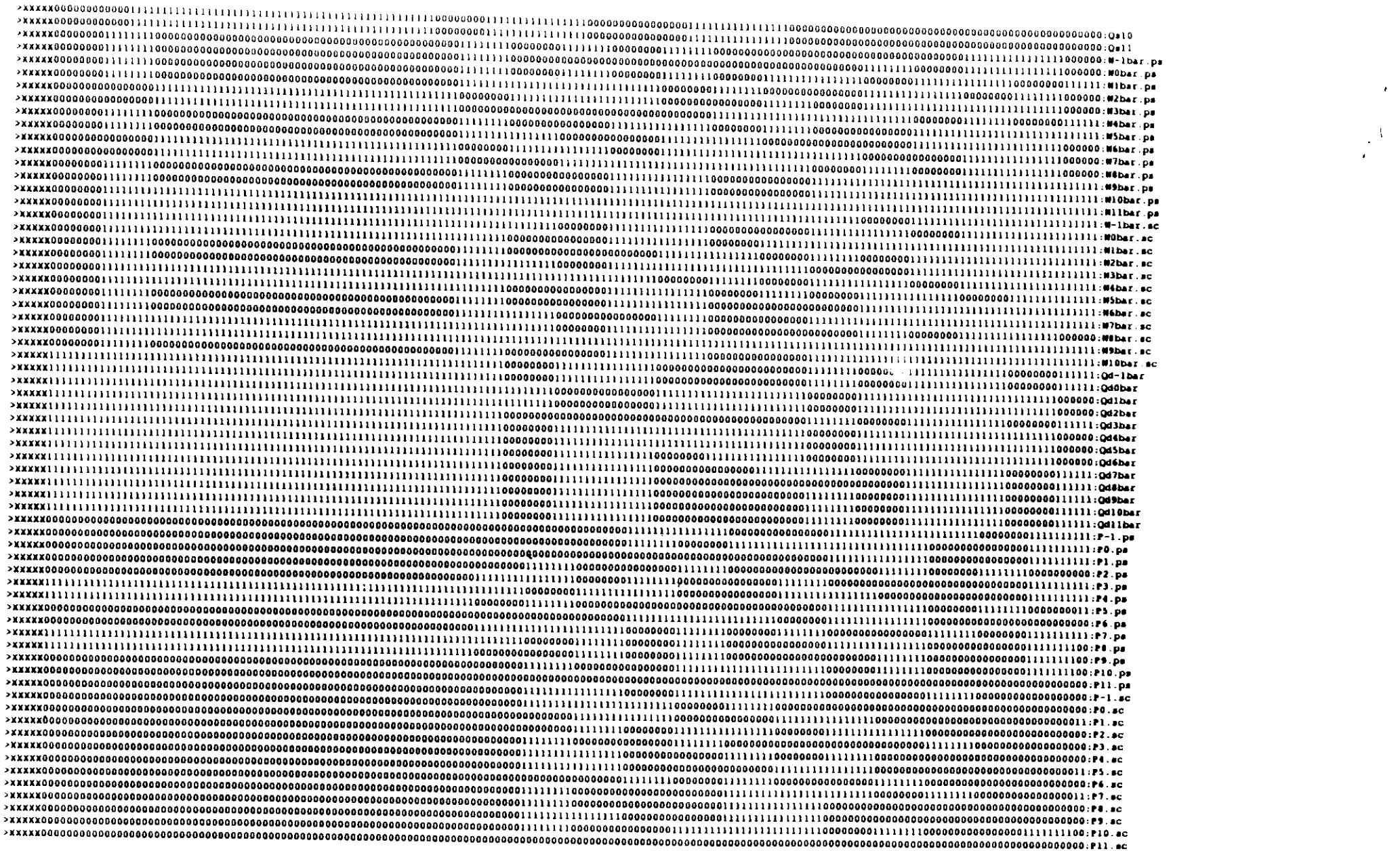
pub3 / Public 3

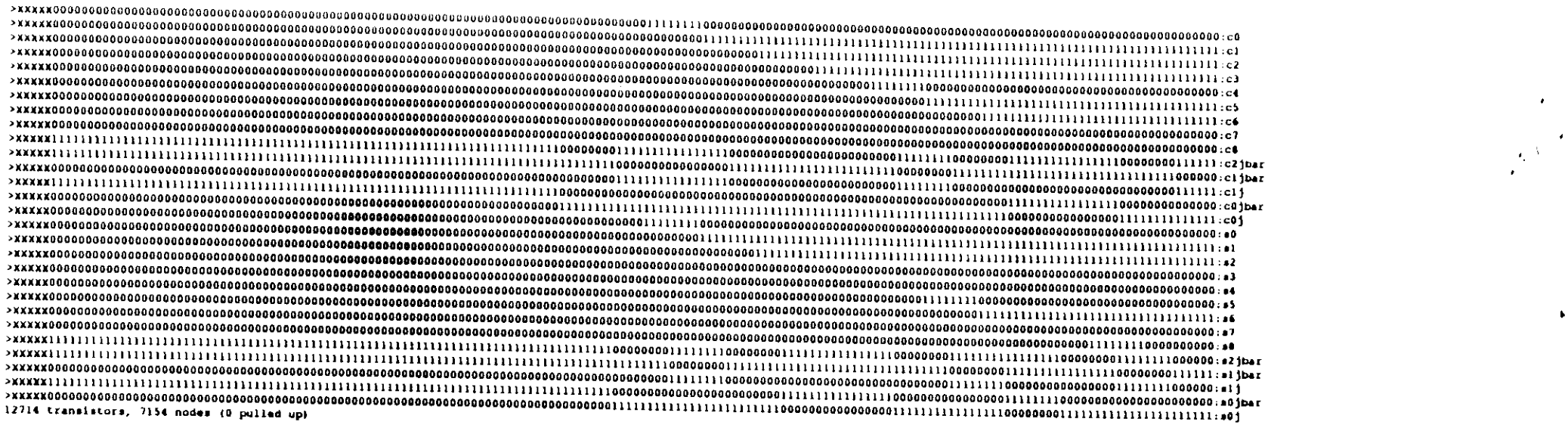
```
pub3 maui:faris  Job: case9.out  Date: Thu Dec 15 00:25:15 1988

pub3 maui:faris  Job: case9.out  Date: Thu Dec 15 00:25:15 1988

pub3 maui:faris  Job: case9.out  Date: Thu Dec 15 00:25:15 1988

pub3 maui:faris  Job: case9.out  Date: Thu Dec 15 00:25:15 1988
```


phi1
phi1bar
phi2
phi2bar
ENABLE
ENABLEbar
GRESET
GRESETbar
etemp3
etemp2
etemp1
etemp0
es3
es2
es1
es0
ec3
ec2
ec1
ec0
zdbar
passGbar
passHbar
shiftG
shiftGbar
shiftH
shiftHbar
xj
yj
xjbar.hold
yjbar.hold
X1
X2
X3
X4
X5
X6
X7
X8
X9
Qx1
Qx2
Qx3
Qx4
Qx5
Qx6
Qx7
Qx8
Qx9
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
Qy1
Qy2
Qy3
Qy4
Qy5
Qy6
Qy7
Qy8









12714 transistors, 7156 nodes (0 pulled up)

maui:faris

case10.out

Thu Dec 15 00:27:37 1988

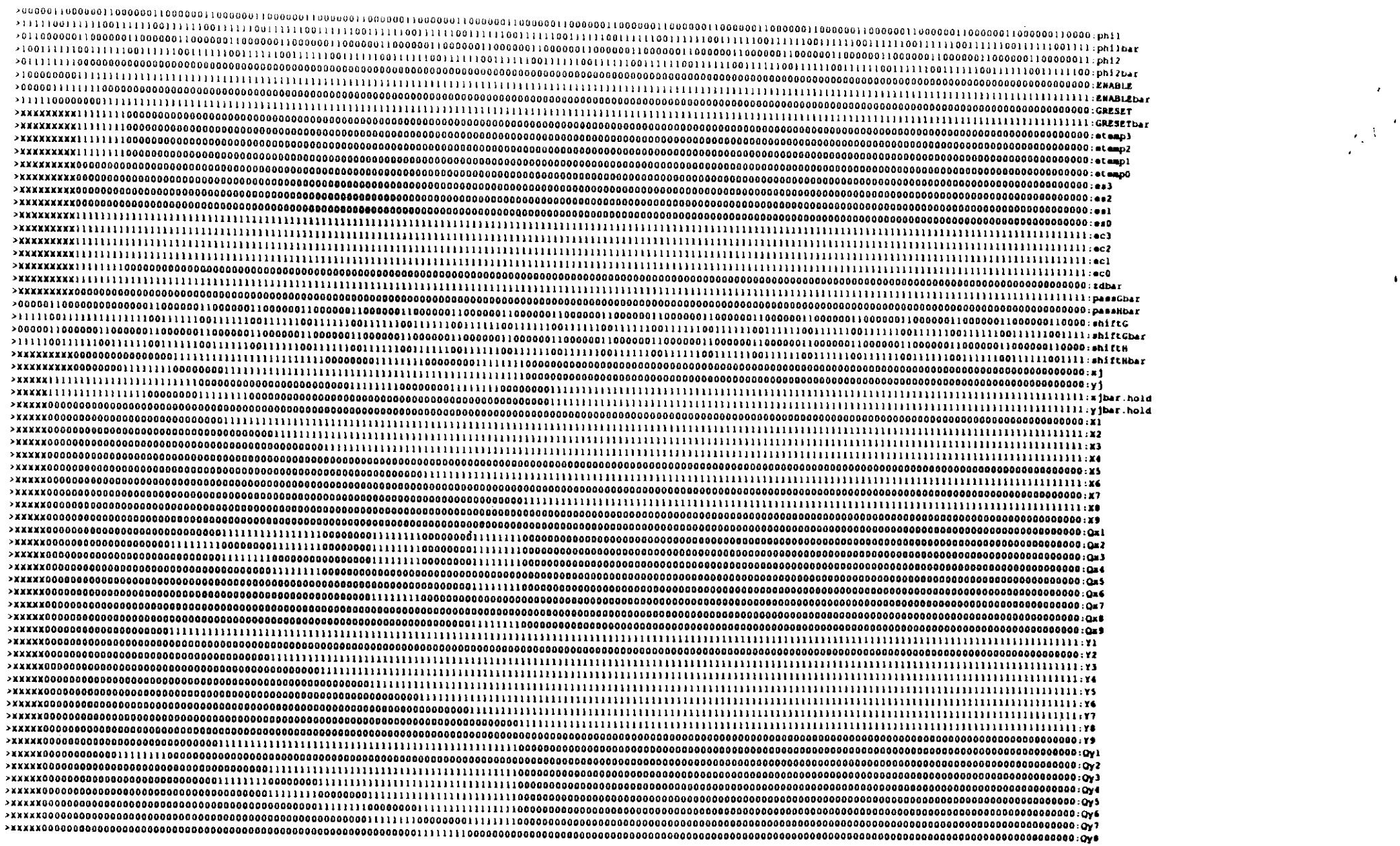
pub3 / Public 3

pub3 maui:faris Job: case10.out Date: Thu Dec 15 00:27:37 1988

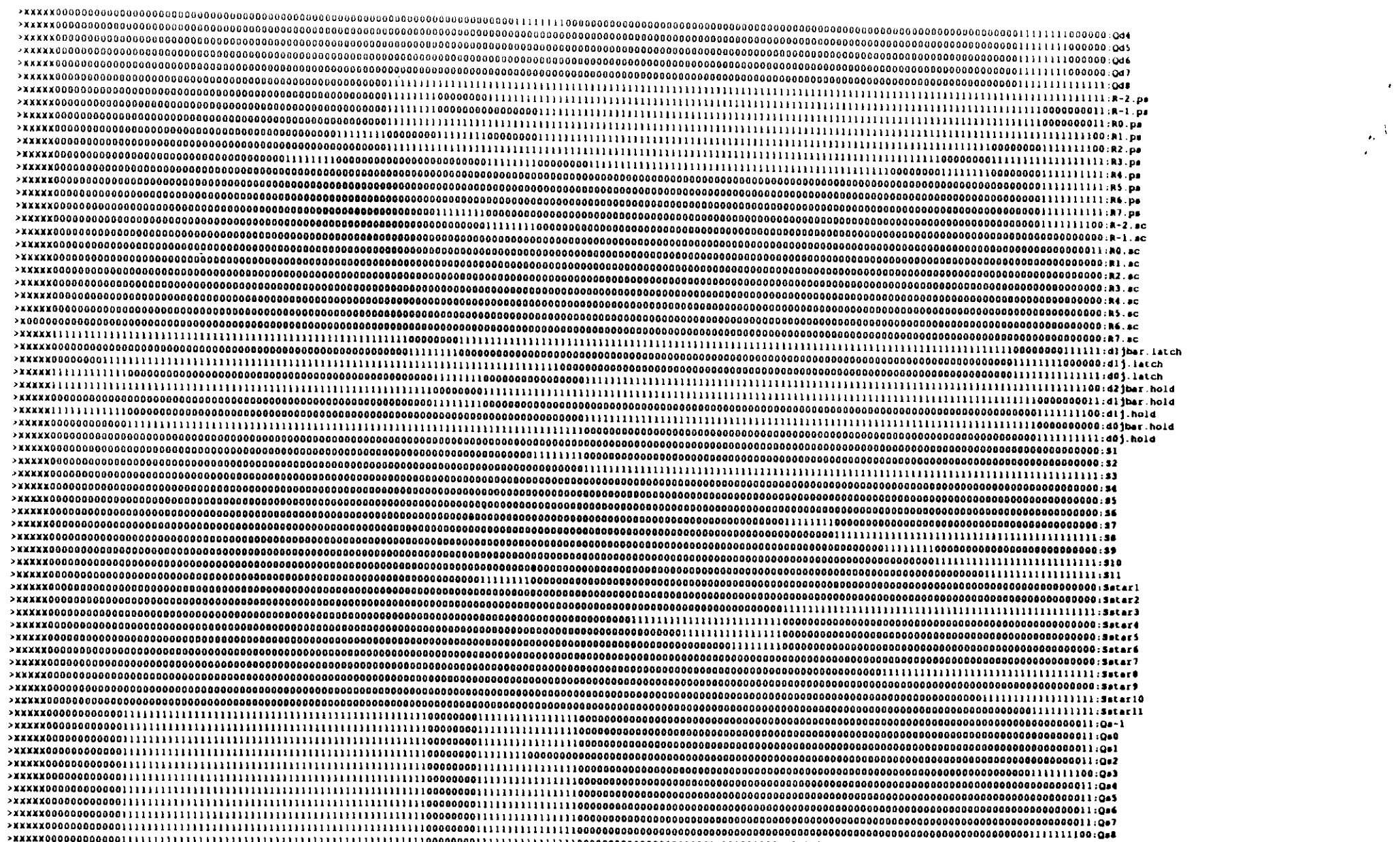
pub3 maui:faris Job: case10.out Date: Thu Dec 15 00:27:37 1988

pub3 maui:faris Job: case10.out Date: Thu Dec 15 00:27:37 1988

pub3 maui:faris Job: case10.out Date: Thu Dec 15 00:27:37 1988


phi1
phi1bar
phi2
phi2bar
ENABLE
ENABLEbar
GRESET
GRESETbar
etemp3
etemp2
etemp1
etemp0
es3
es2
es1
es0
ec3
ec2
ec1
ec0
zdbar
passGbar
passHbar
shiftG
shiftGbar
shiftH
shiftHbar
xj
yj
xjbar.hold
yjbar.hold
X1
X2
X3
X4
X5
X6
X7
X8
X9
Qx1
Qx2
Qx3
Qx4
Qx5
Qx6
Qx7
Qx8
Qx9
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
Qy1
Qy2
Qy3
Qy4
Qy5
Qy6
Qy7
Qy8

Dy9
M-1_ps
M0_ps
M1_ps
M2_ps
M3_ps
M4_ps
M5_ps
M6_ps
M7_ps
M8_ps
M-1_sc
M0_sc
M1_sc
M2_sc
M3_sc
M4_sc
M5_sc
M6_sc
M7_sc
z2bar
z1bar
z0bar
E-2
E-1
E0
E1
E2
E3
E4
E5
E6
E7
D0bar
D1bar
D2bar
D3bar
D4bar
D5bar
D6bar
D7bar
D8bar
D0
D1
D2
D3
D4
D5
D6
D7
D8
Datar0
Datar1
Datar2
Datar3
Datar4
Datar5
Datar6
Datar7
Datar8
Q-1
Q0
Q1
Q2
Q3


Qd4
Qd5
Qd6
Qd7
Qd8
R-2.ps
R-1.ps
R0.ps
R1.ps
R2.ps
R3.ps
R4.ps
R5.ps
R6.ps
R7.ps
R-2.sc
R-1.sc
R0.sc
R1.sc
R2.sc
R3.sc
R4.sc
R5.sc
R6.sc
R7.sc
d1jbar.latch
d1j.latch
d0j.latch
d2jbar.hold
d1jbar.hold
d1j.hold
d0jbar.hold
d0j.hold
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
Sstar1
Sstar2
Sstar3
Sstar4
Sstar5
Sstar6
Sstar7
Sstar8
Sstar9
Sstar10
Sstar11
Qs-1
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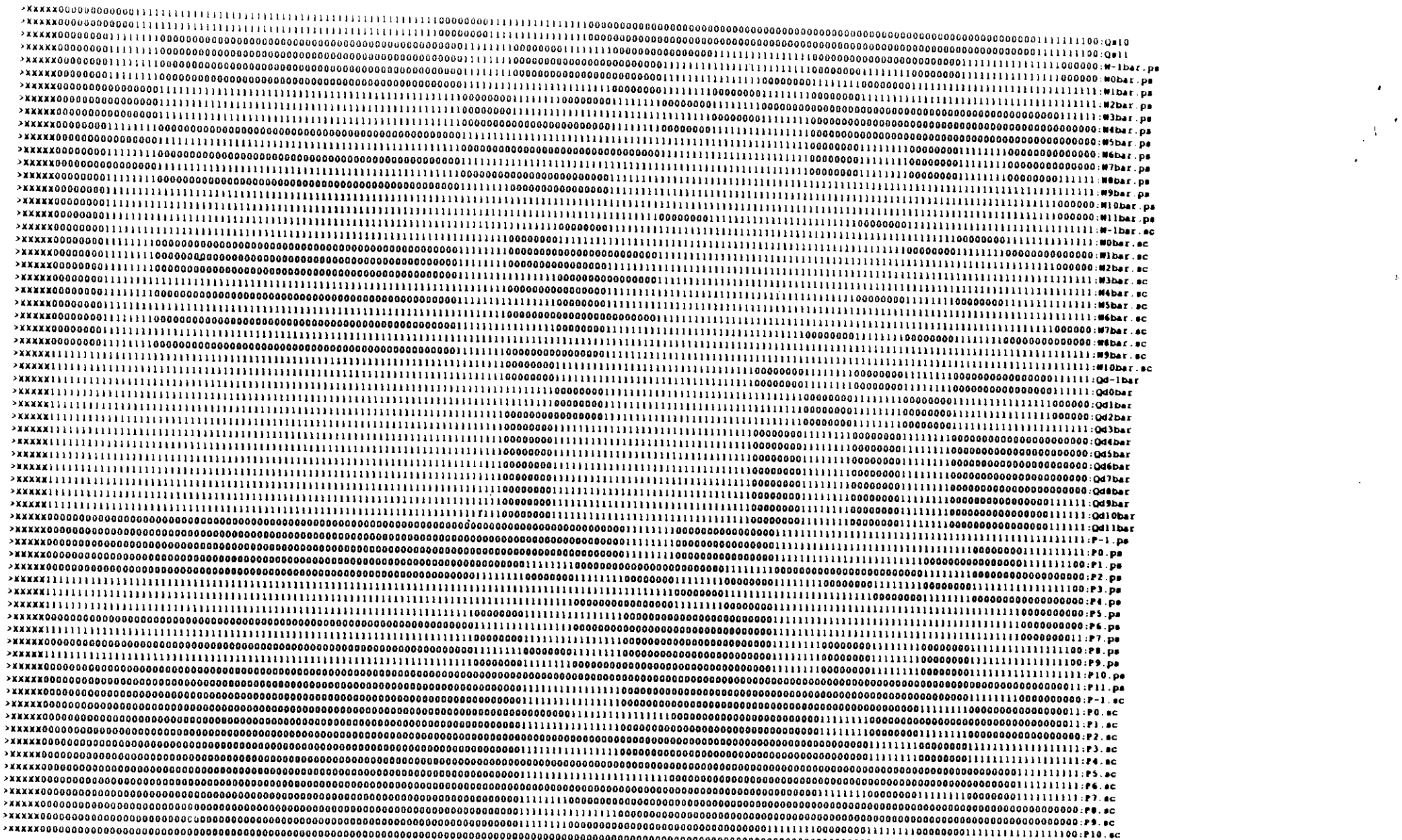
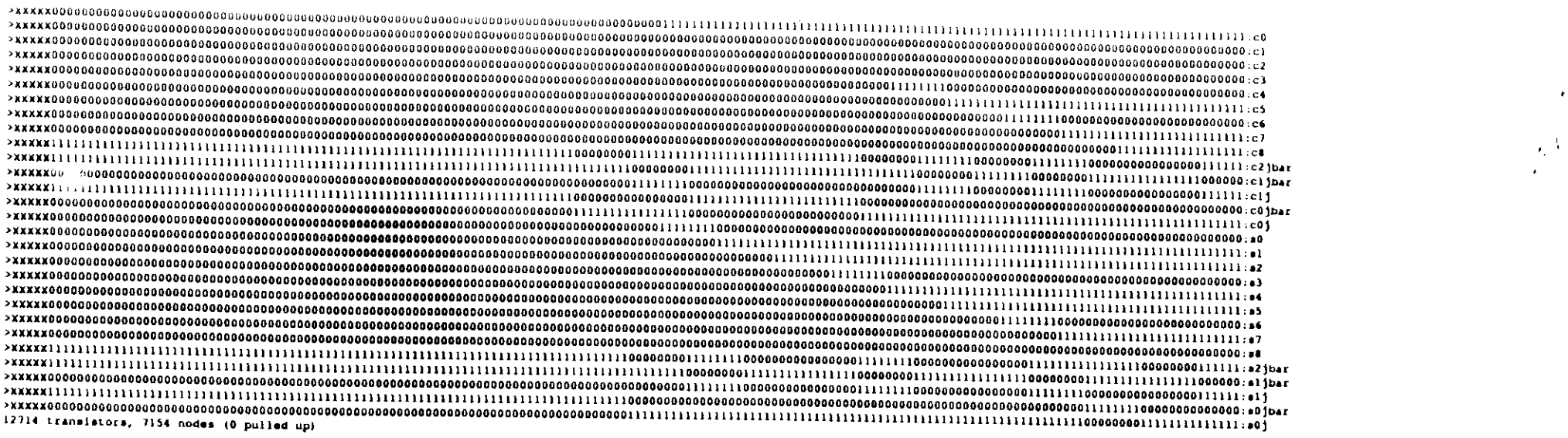
Qs1
Qs2
Qs3
Qs4
Qs5
Qs6
Qs7
Qs8
Qs9




12714 transistors, 7154 nodes (0 pulled up)

maui:faris

case11.out

Sat Dec 17 02:07:01 1988

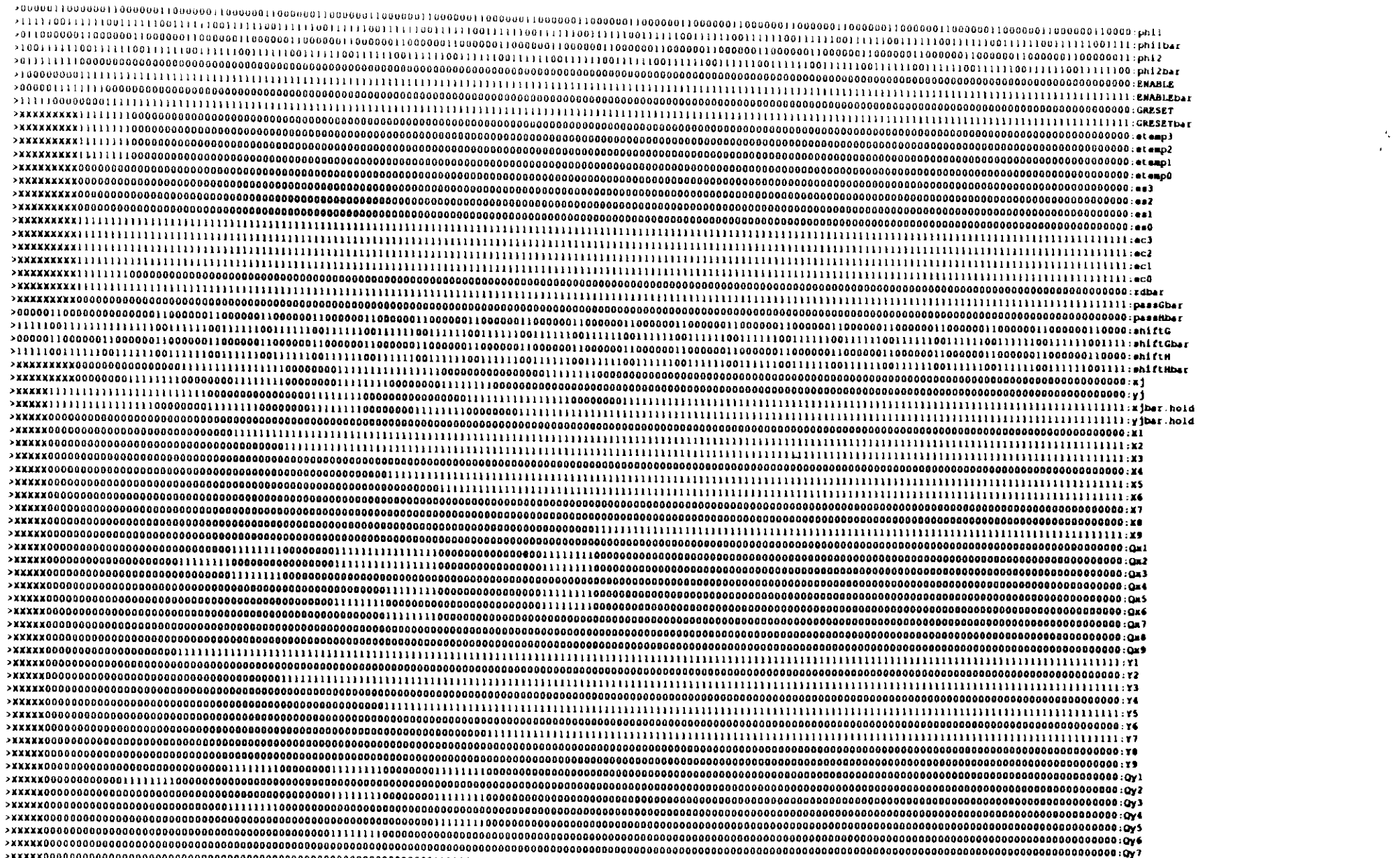
pub3 / Public 3

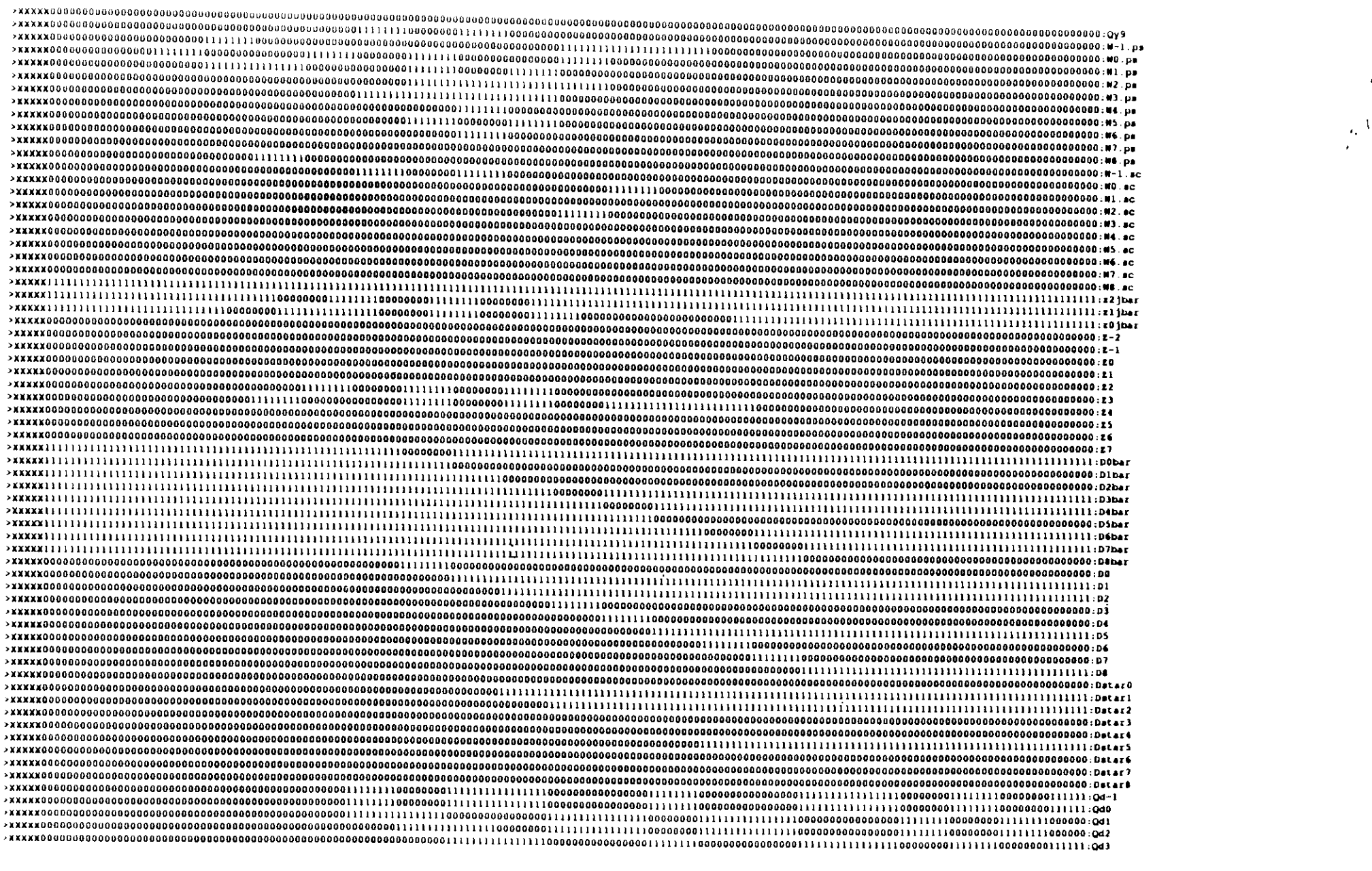
pub3 maui:faris Job: case11.out Date: Sat Dec 17 02:07:01 1988

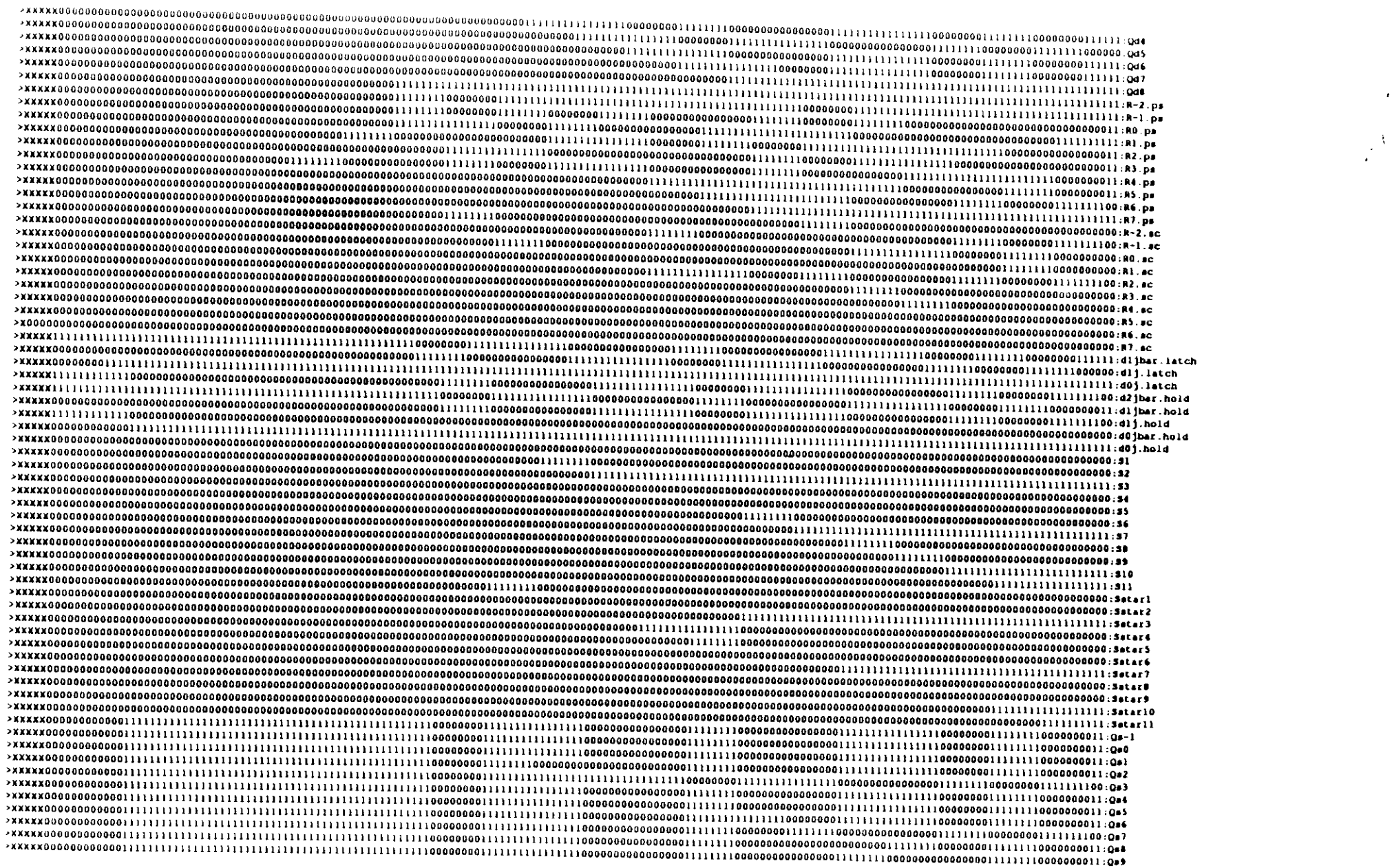
pub3 maui:faris Job: case11.out Date: Sat Dec 17 02:07:01 1988

pub3 maui:faris Job: case11.out Date: Sat Dec 17 02:07:01 1988

pub3 maui:faris Job: case11.out Date: Sat Dec 17 02:07:01 1988


phi1
phi1bar
phi2
phi2bar
ENABLE
ENABLEbar
GRESET
GRESETbar
etemp3
etemp2
etemp1
etemp0
es3
es2
es1
es0
ec3
ec2
ec1
ec0
rdbar
passGbar
passHbar
shiftG
shiftGbar
shiftH
shiftHbar
xj
yj
xjbar.hold
yjbar.hold
X1
X2
X3
X4
X5
X6
X7
X8
X9
Qx1
Qx2
Qx3
Qx4
Qx5
Qx6
Qx7
Qx8
Qx9
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
Qy1
Qy2
Qy3
Qy4
Qy5
Qy6
Qy7
Qy8


Qy9
W-1.ps
W0.ps
W1.ps
W2.ps
W3.ps
W4.ps
W5.ps
W6.ps
W7.ps
W8.ps
W-1.sc
W0.sc
W1.sc
W2.sc
W3.sc
W4.sc
W5.sc
W6.sc
W7.sc
W8.sc
z2jbar
z1jbar
z0jbar
Z-2
Z-1
Z0
Z1
Z2
Z3
Z4
Z5
Z6
Z7
D0bar
D1bar
D2bar
D3bar
D4bar
D5bar
D6bar
D7bar
D8bar
D0
D1
D2
D3
D4
D5
D6
D7
D8
Dstar0
Dstar1
Dstar2
Dstar3
Dstar4
Dstar5
Dstar6
Dstar7
Dstar8
Qd-1
Qd0
Qd1
Qd2
Qd3


Qd4
Qd5
Qd6
Qd7
Qd8
R-2.ps
R-1.ps
R0.ps
R1.ps
R2.ps
R3.ps
R4.ps
R5.ps
R6.ps
R7.ps
R-2.sc
R-1.sc
R0.sc
R1.sc
R2.sc
R3.sc
R4.sc
R5.sc
R6.sc
R7.sc
d1jbar.latch
d1j.latch
d0j.latch
d2jbar.hold
d1jbar.hold
d1j.hold
d0jbar.hold
d0j.hold
$1
$2
$3
$4
$5
$6
$7
$8
$9
$10
$11
$star1
$star2
$star3
$star4
$star5
$star6
$star7
$star8
$star9
$star10
$star11
Qs-1
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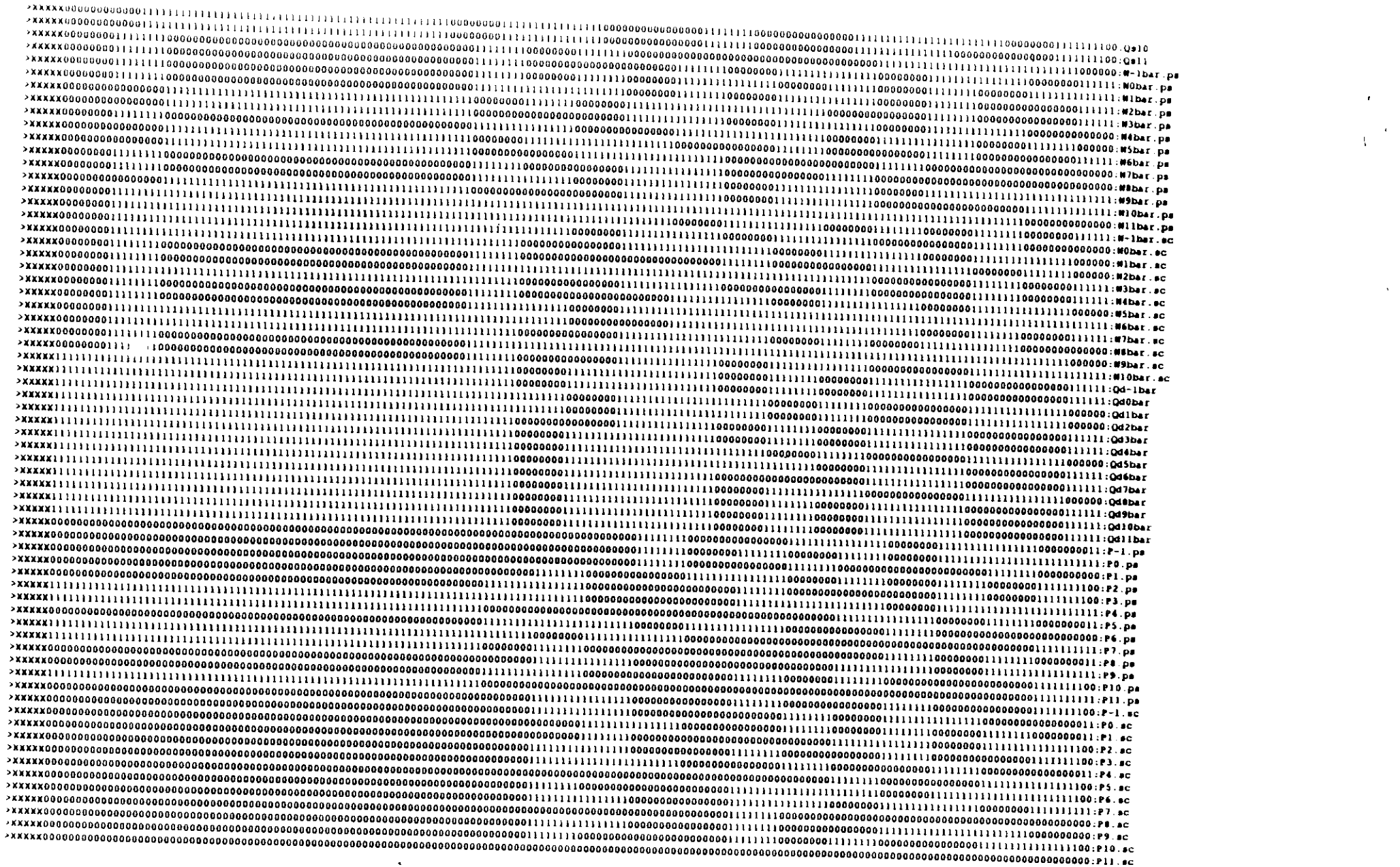
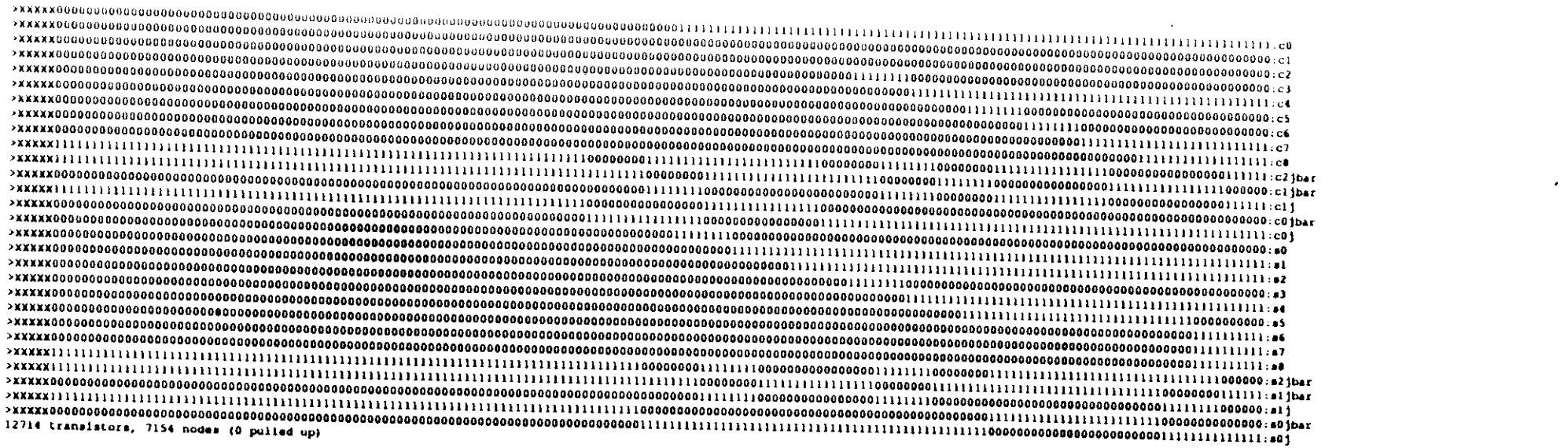
Qs4
Qs5
Qs6
Qs7
Qs8
Qs9





12714 translators, 7154 nodes (0 pulled up)

maui:faris

case12.out

Thu Dec 15 00:34:30 1988

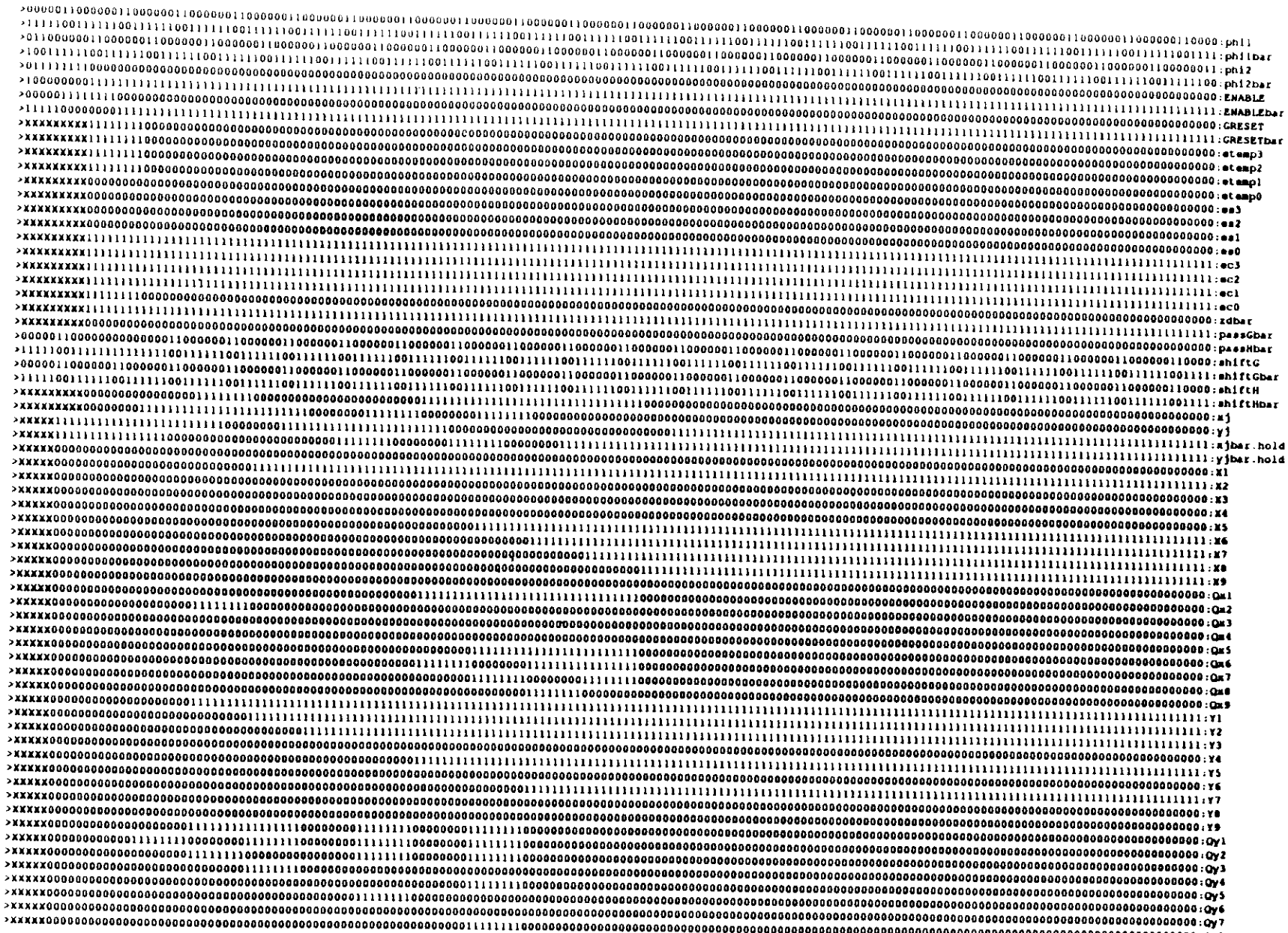
pub3 / Public 3

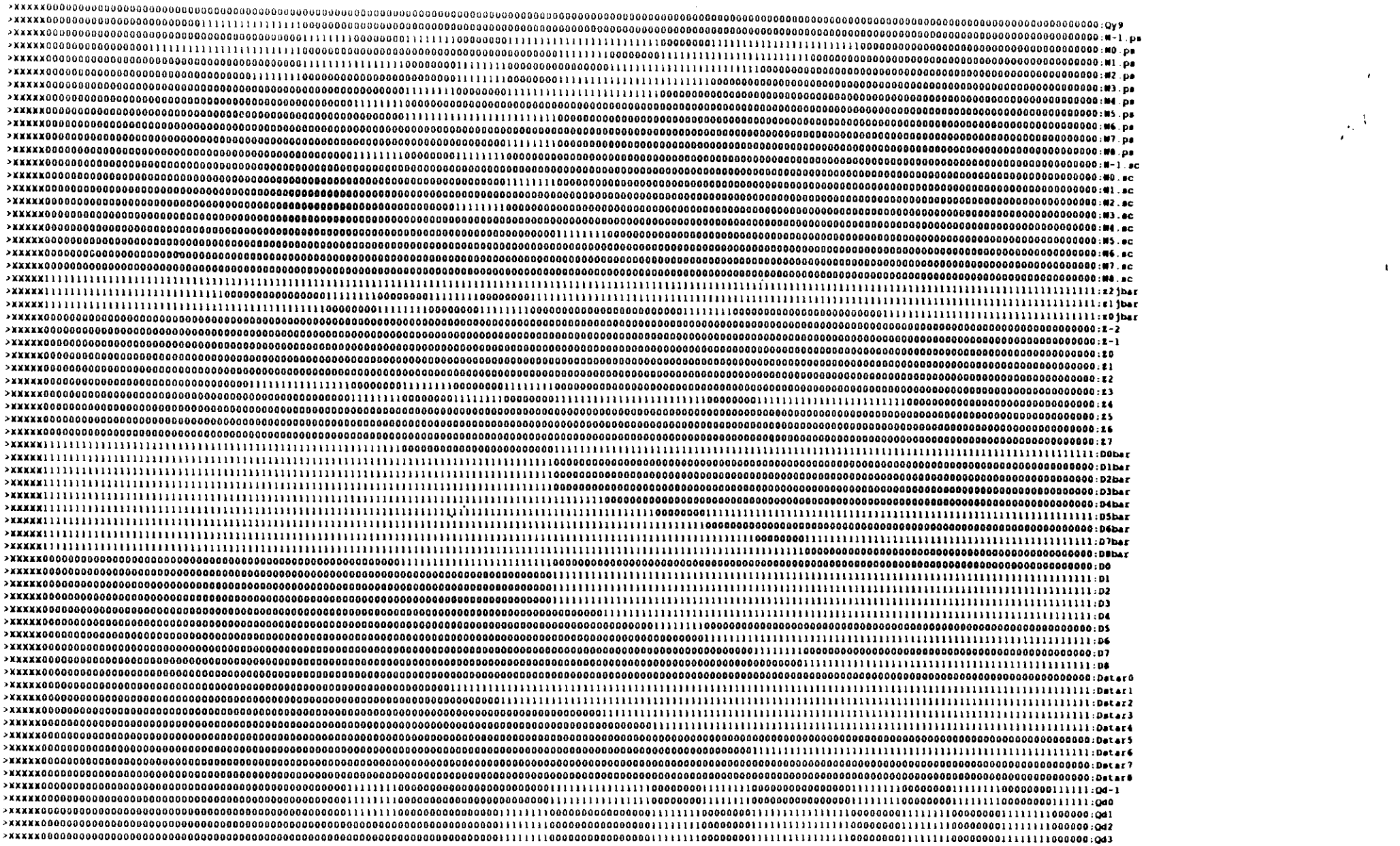
pub3 maui:faris Job: case12.out Date: Thu Dec 15 00:34:30 1988

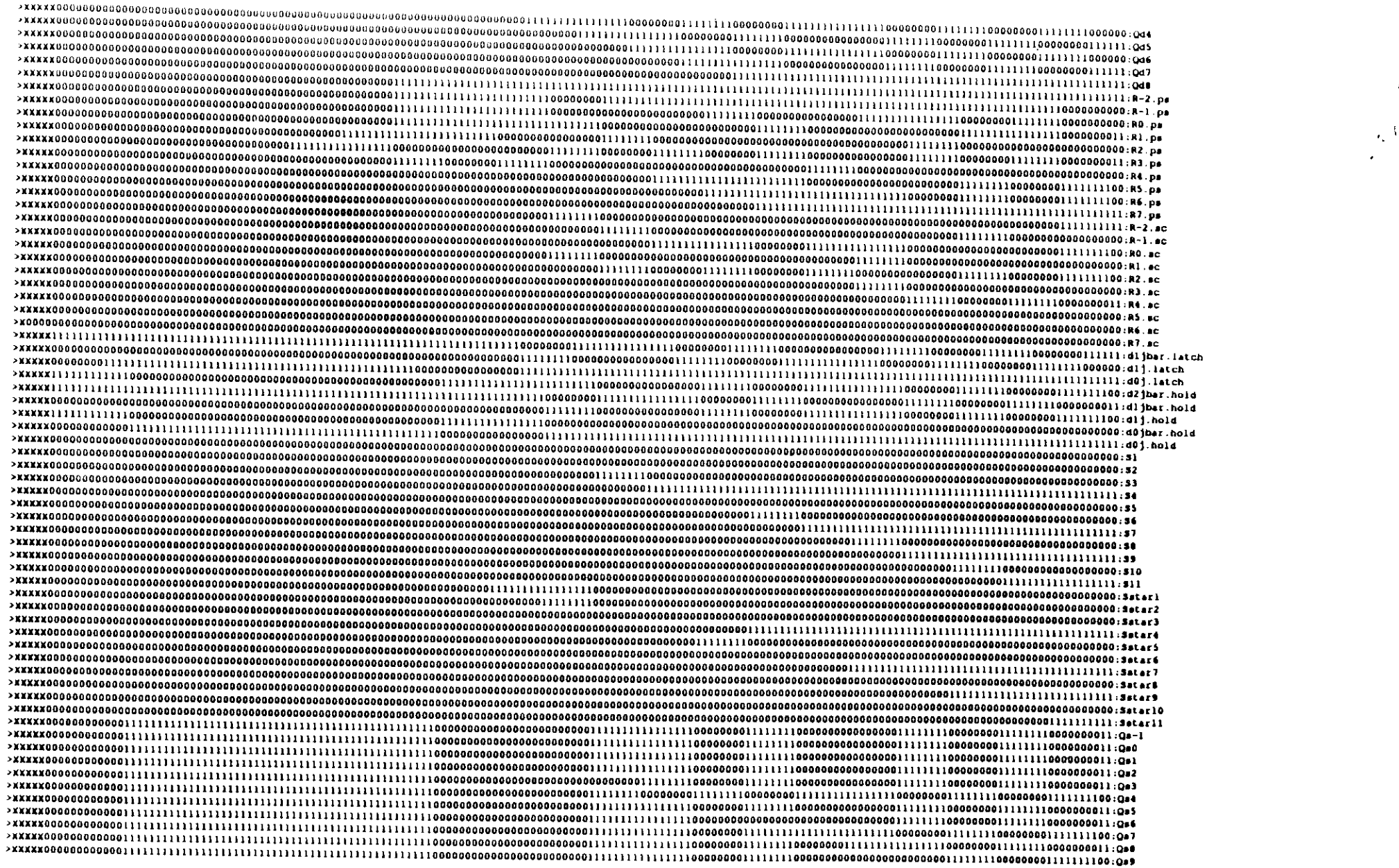
pub3 maui:faris Job: case12.out Date: Thu Dec 15 00:34:30 1988

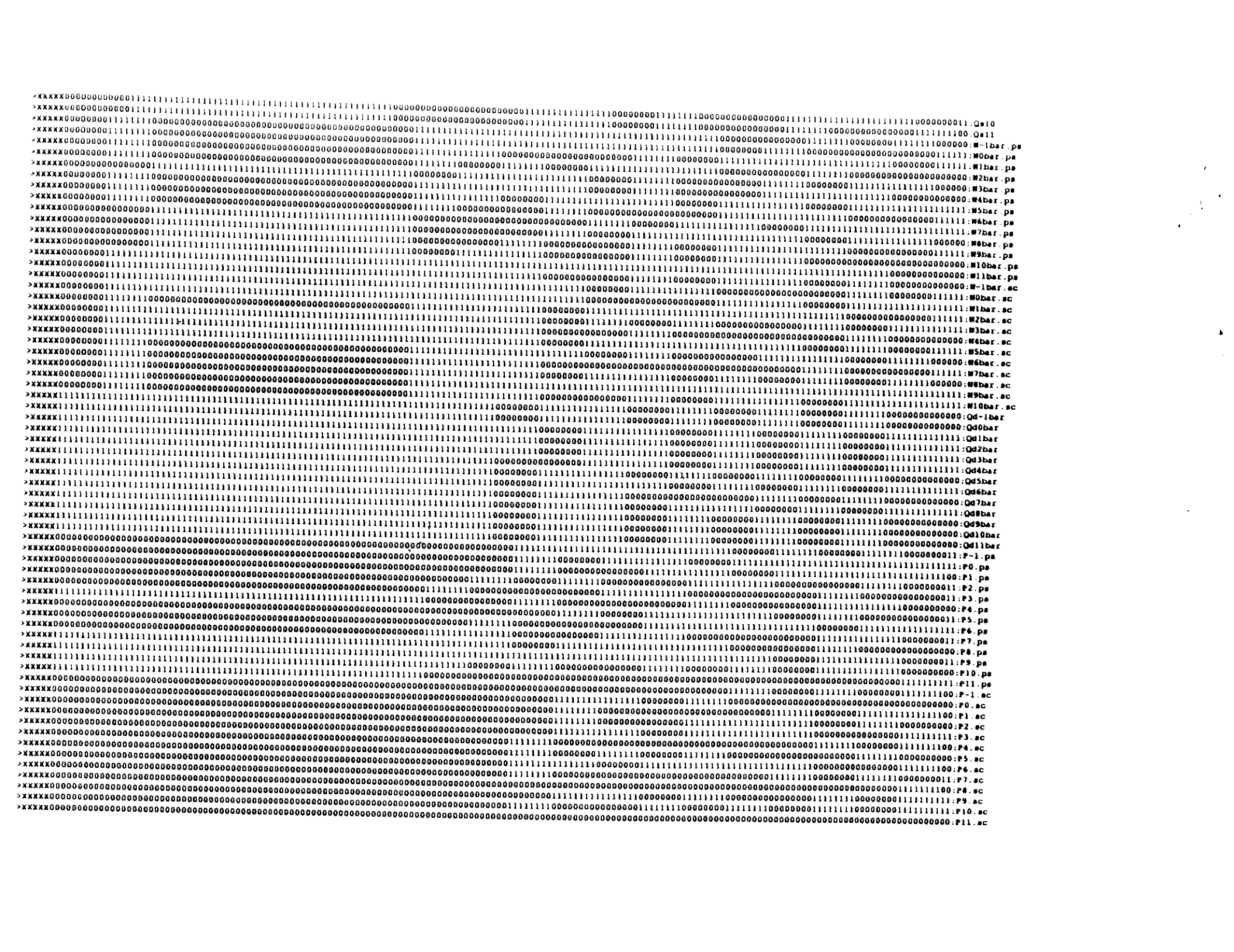
pub3 maui:faris Job: case12.out Date: Thu Dec 15 00:34:30 1988

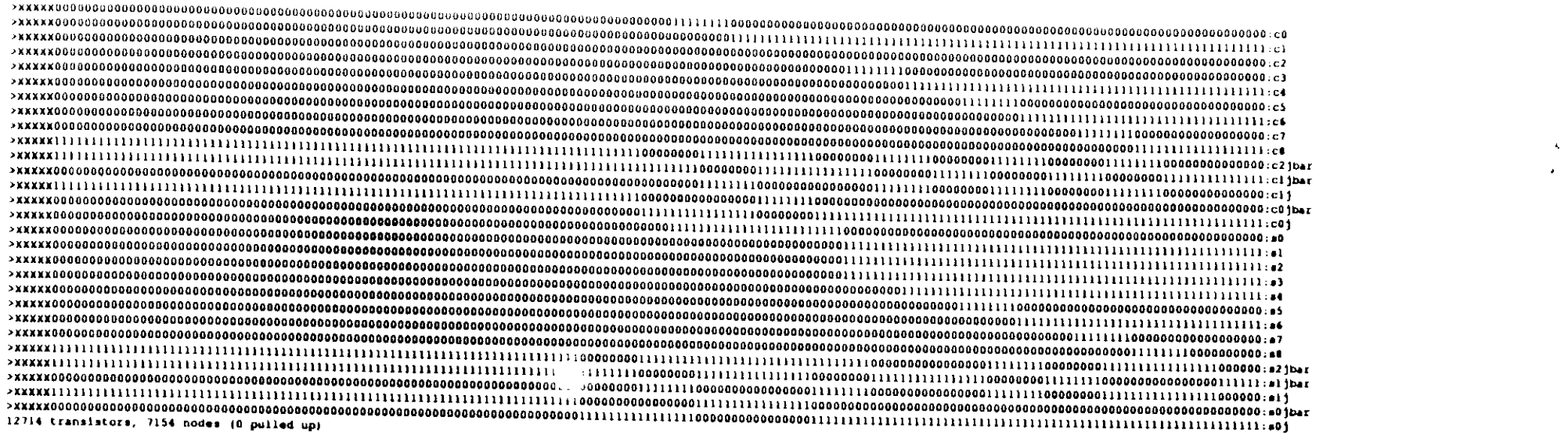
pub3 maui:faris Job: case12.out Date: Thu Dec 15 00:34:30 1988


phi1
phi1bar
phi2
phi2bar
ENABLE
ENABLEbar
GRESET
GRESETbar
etemp3
etemp2
etemp1
etemp0
es3
es2
es1
es0
ec3
ec2
ec1
ec0
xdbar
passGbar
passHbar
shiftG
shiftGbar
shiftH
shiftHbar
xj
yj
xjbar.hold
yjbar.hold
X1
X2
X3
X4
X5
X6
X7
X8
X9
Qx1
Qx2
Qx3
Qx4
Qx5
Qx6
Qx7
Qx8
Qx9
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
Qy1
Qy2
Qy3
Qy4
Qy5
Qy6
Qy7
Qy8


Qy9
M-1.ps
M0.ps
M1.ps
M2.ps
M3.ps
M4.ps
M5.ps
M6.ps
M7.ps
M8.ps
M-1.sc
M0.sc
M1.sc
M2.sc
M3.sc
M4.sc
M5.sc
M6.sc
M7.sc
M8.sc
z2jbar
z1jbar
z0jbar
Z-2
Z-1
Z0
Z1
Z2
Z3
Z4
Z5
Z6
Z7
D0bar
D1bar
D2bar
D3bar
D4bar
D5bar
D6bar
D7bar
D8bar
D0
D1
D2
D3
D4
D5
D6
D7
D8
Dstar0
Dstar1
Dstar2
Dstar3
Dstar4
Dstar5
Dstar6
Dstar7
Dstar8
Qd-1
Qd0
Qd1
Qd2
Qd3



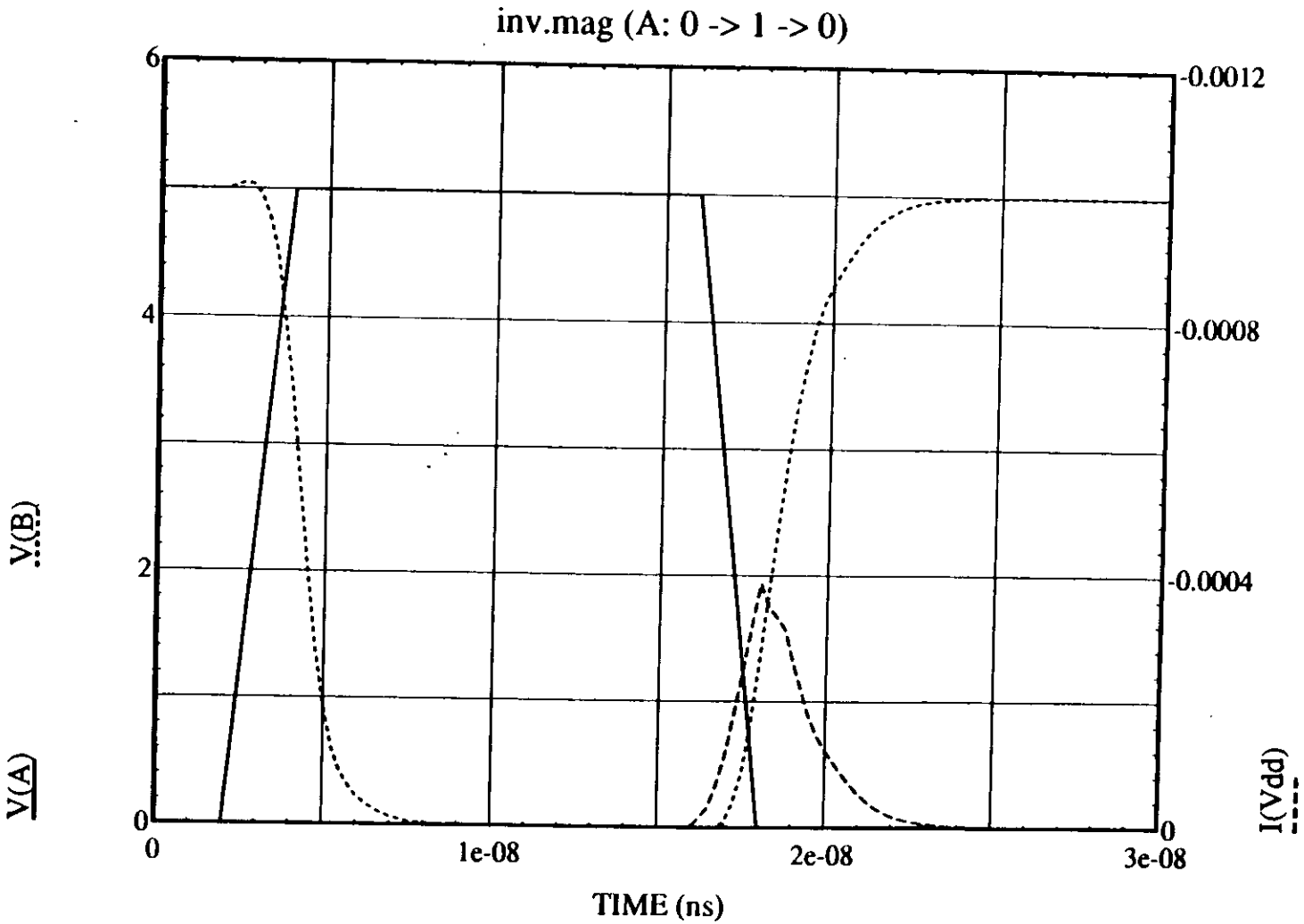



12714 transistors, 7154 nodes (0 pulled up)

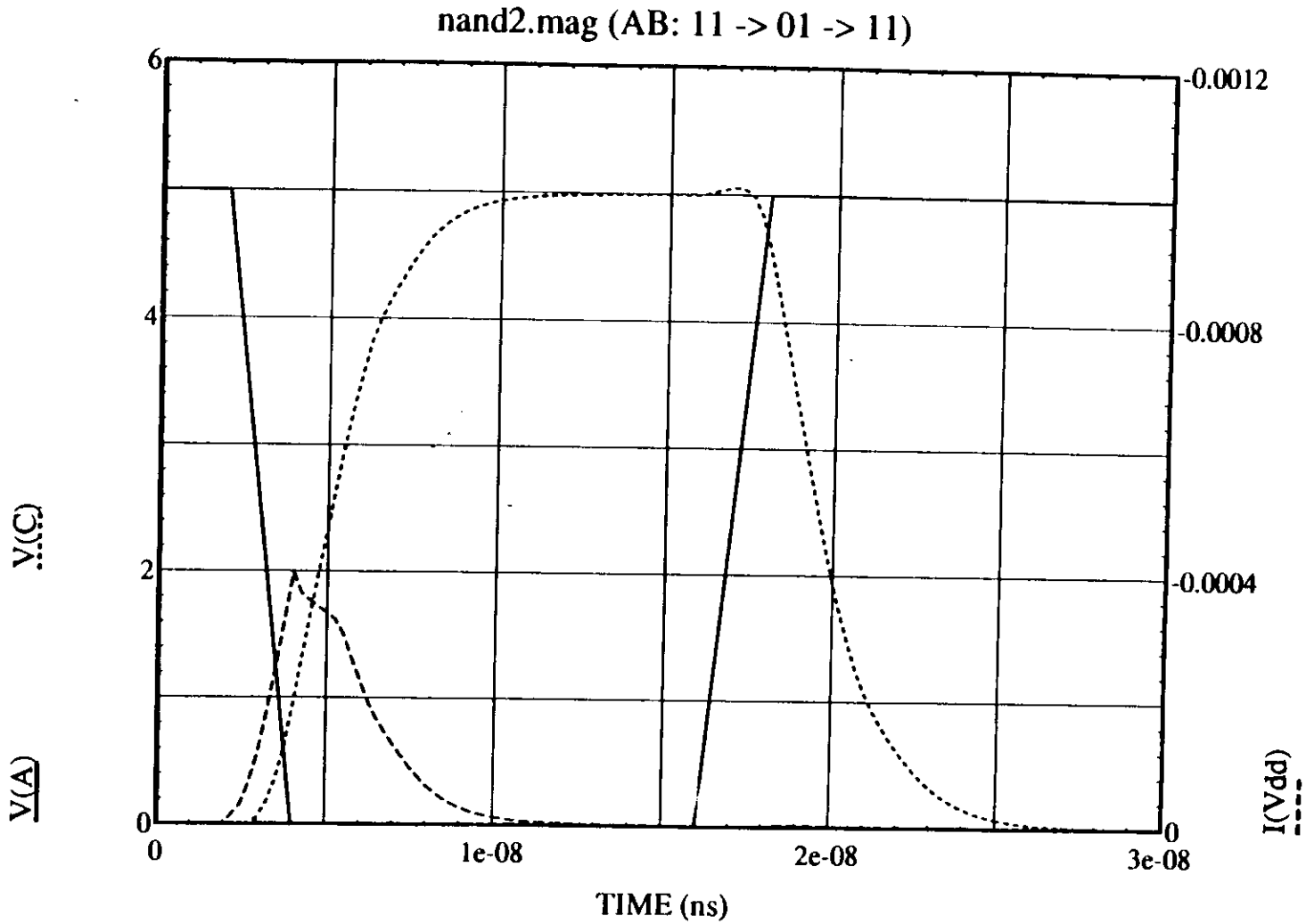
2.1 Spice Results: Standard Cells (All Input Combinations)

```
set GND         0
set Vdd         1
set Vload       2
set CMOSP       4
set CMOSN       5

set CLK         10
set CLKbar      11
set CLKM        12
set CLKMbar     13
set CLKS        14
set CLKSbar     15
set PRESET      16

set A           20
set B           21
set C           22
set D           23
set D0          24
set D1          25
set S           26
set Sbar        27
set shiftin     28
set shiftin0    29

set CYbar       40
set SUMbar      41
set Q           42
set Qbar        43
set QM          44
set QMbar       45
set QS          46
set QSbar       47
```

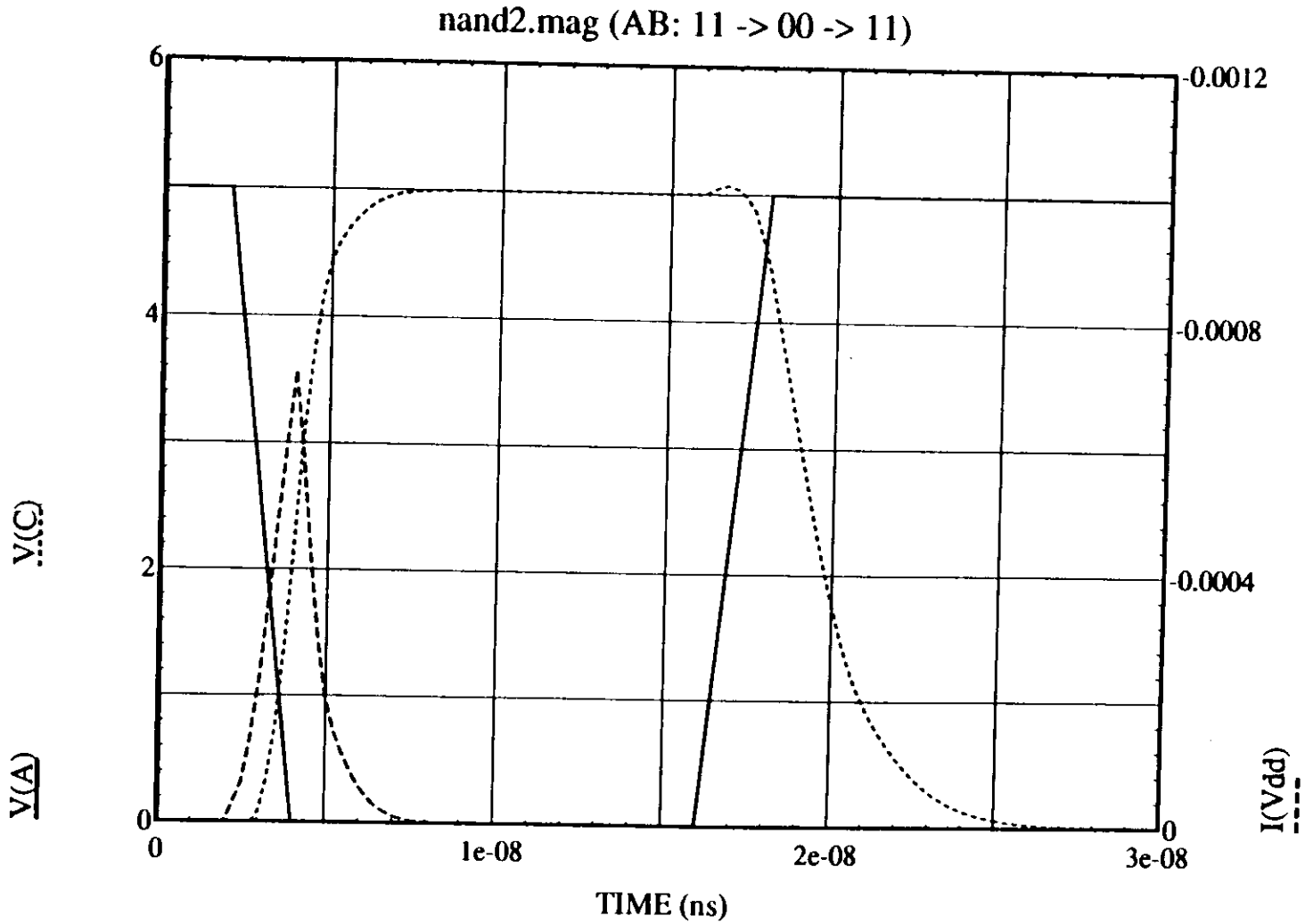
```
*  Simulation of cell:  inv.mag (A: 0 -> 1 -> 0)                    HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,12ns)
define(TF,2ns)
define(TL,12ns)
define(PER,28ns)
define(TIME,30ns)
*
*
*     _____________
*    /             \
*___/       A       \_____________
*                                                                  HERE
VA  20  0  pulse(0 5 TD TR TF TH PER)
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*                                                                  HERE
.tran 0.25ns TIME
.print trans v(20) v(21) i(Vdd)
.print trans v(100)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit input (= load)
*  Passing Vload Vcmosp Vcmosn output subcktname
*                                                                  HERE
XLOAD 2 4 5 21 100 load
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*                                                                  HERE
include(/ics12/dloh/spice.dir/inv.dir/inv.spice)
*
include(/ics12/dloh/spice.dir/models)
*
.end
```


inv.mag (A: 0 -> 1 -> 0)
6
4
2
0
-0.0012
-0.0008
-0.0004
0
0
1e-08
2e-08
3e-08
TIME (ns)
V(A)
V(B)
I(Vdd)

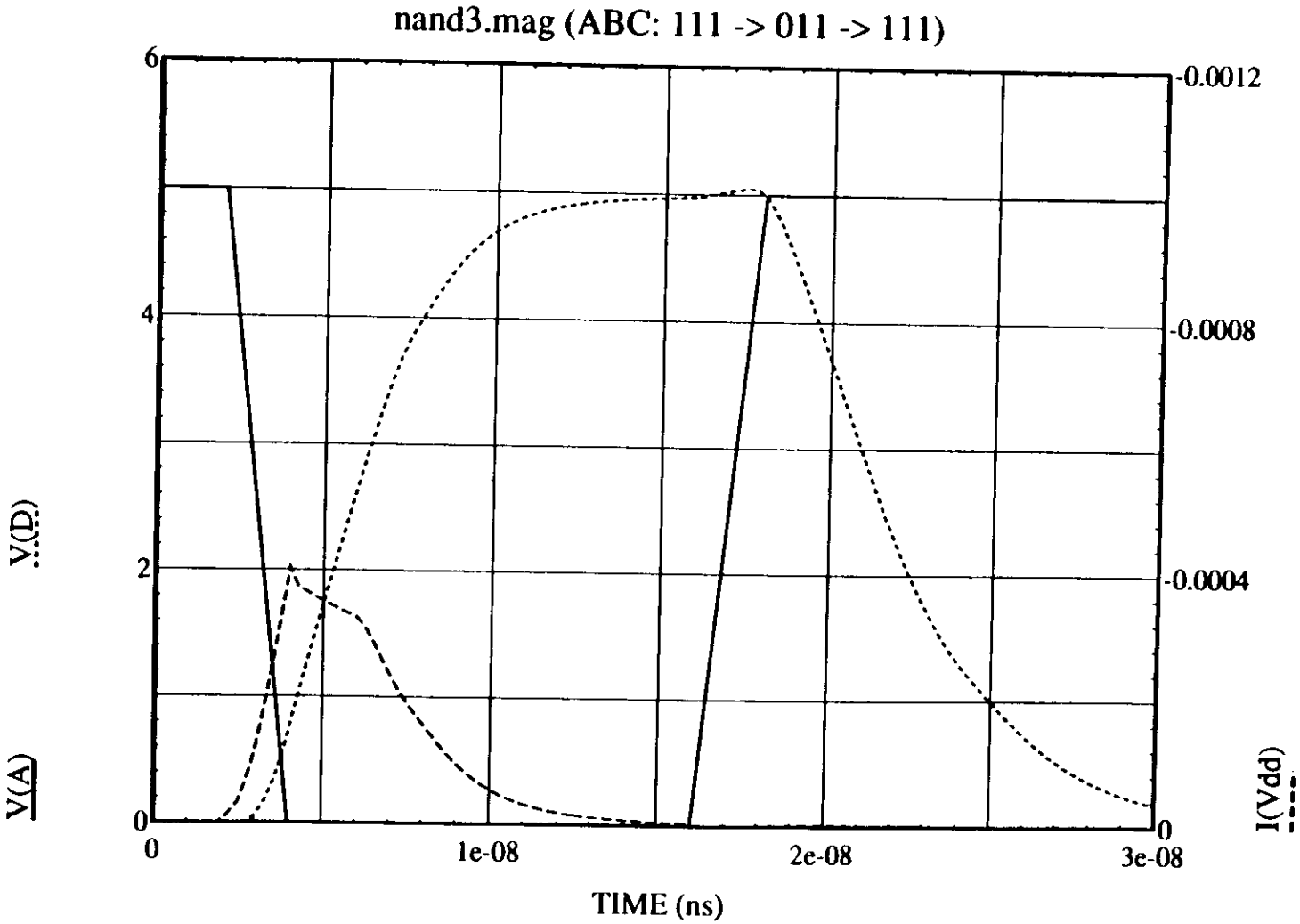
```
*  Simulation of cell:  nand2.mag (AB: 11 -> 01 -> 11)      HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,12ns)
define(TF,2ns)
define(TL,12ns)
define(PER,28ns)
define(TIME,30ns)
*
*
*___
*   \       A       /____________
*    \______________/
*                                                          HERE
VA  20  0  pulse(5 0 TD TR TF TH PER)
VB  21  0  5V
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*                                                          HERE
.tran 0.25ns TIME
.print trans v(20) v(22) i(Vdd)
.print trans v(100)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit input (= load)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
*                                                          HERE
XLOAD 2 4 5 22 100 load
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*                                                          HERE
include(/ics12/dloh/spice.dir/nand2.dir/nand2.spice)
*
include(/ics12/dloh/spice.dir/models)
*
.end
```


nand2.mag (AB: 11 -> 01 -> 11)
6
4
2
0
-0.0012
-0.0008
-0.0004
0
0
1e-08
2e-08
3e-08
TIME (ns)
V(A)
V(C)
I(Vdd)

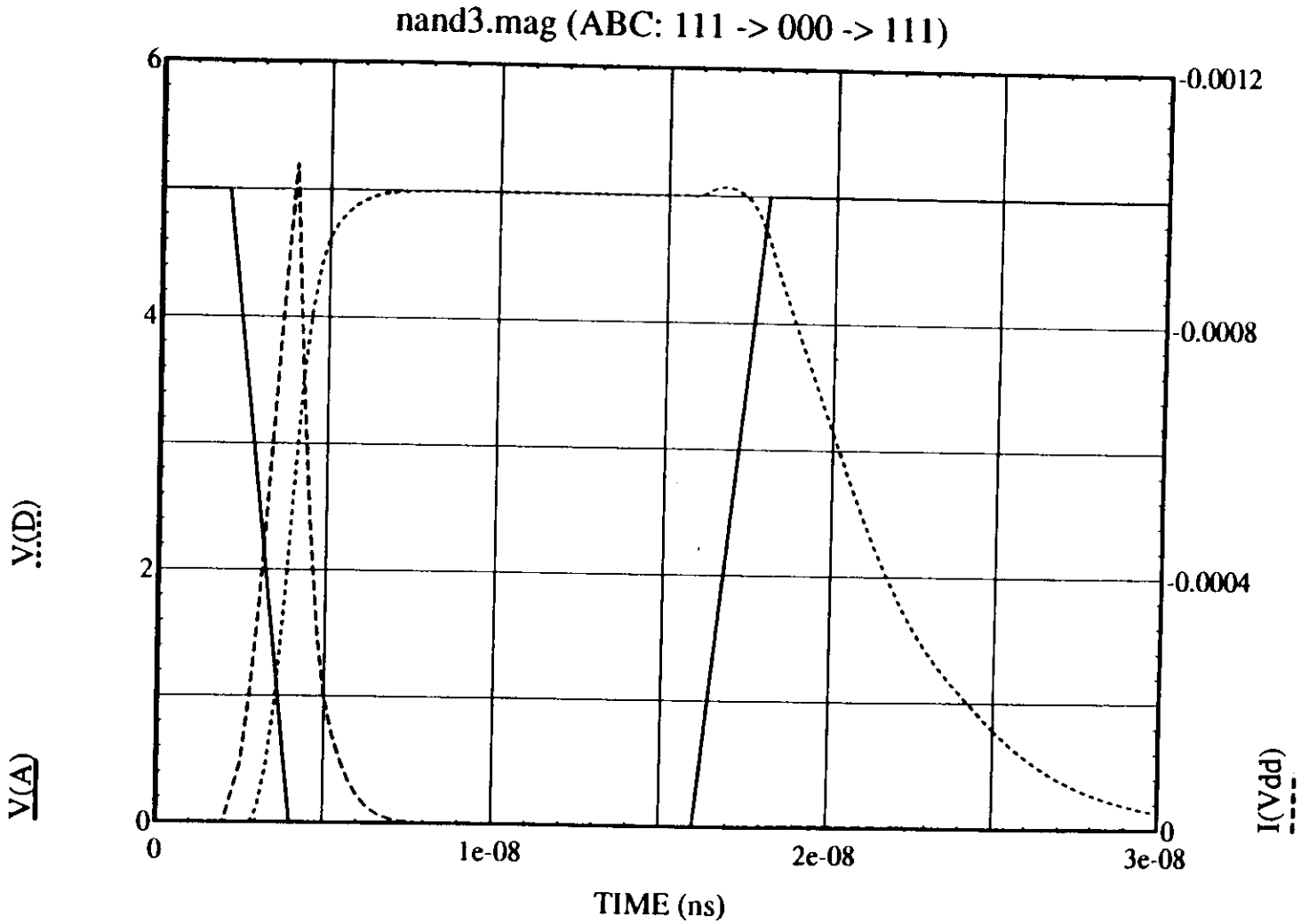
```
*  Simulation of cell:  nand2.mag (AB: 11 -> 00 -> 11)      HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,12ns)
define(TF,2ns)
define(TL,12ns)
define(PER,28ns)
define(TIME,30ns)
*
*
*___    \       A       /____________
*    \_____________/
*
*___    \       B       /____________
*    \_____________/
*
VA  20  0  pulse(5 0 TD TR TF TH PER)                    HERE
VB  21  0  pulse(5 0 TD TR TF TH PER)
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*
.tran 0.25ns TIME                                        HERE
.print trans v(20) v(22) i(Vdd)
.print trans v(100)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit input (= load)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
*
XLOAD 2 4 5 22 100 load                                  HERE
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*
include(/ics12/dloh/spice.dir/nand2.dir/nand2.spice)     HERE
*
include(/ics12/dloh/spice.dir/models)
*
.end
```


nand2.mag (AB: 11 -> 00 -> 11)
6
4
2
0
-0.0012
-0.0008
-0.0004
0
0
1e-08
2e-08
3e-08
TIME (ns)
V(C)
V(A)
I(Vdd)

```
*  Simulation of cell:  nand3.mag (ABC: 111 -> 011 -> 111)      HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,12ns)
define(TF,2ns)
define(TL,12ns)
define(PER,28ns)
define(TIME,30ns)
*
*
*___
*    \       A        /_____________
*     \_____________/
*
VA  20  0  pulse(5 0 TD TR TF TH PER)                          HERE
VB  21  0  5V
VC  22  0  5V
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*
.tran 0.25ns TIME                                              HERE
.print trans v(20) v(23) i(Vdd)
.print trans v(100)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit input (= load)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
*
XLOAD 2 4 5 23 100 load                                        HERE
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*
include(/ics12/dloh/spice.dir/nand3.dir/nand3.spice)           HERE
*
include(/ics12/dloh/spice.dir/models)
*
.end
```

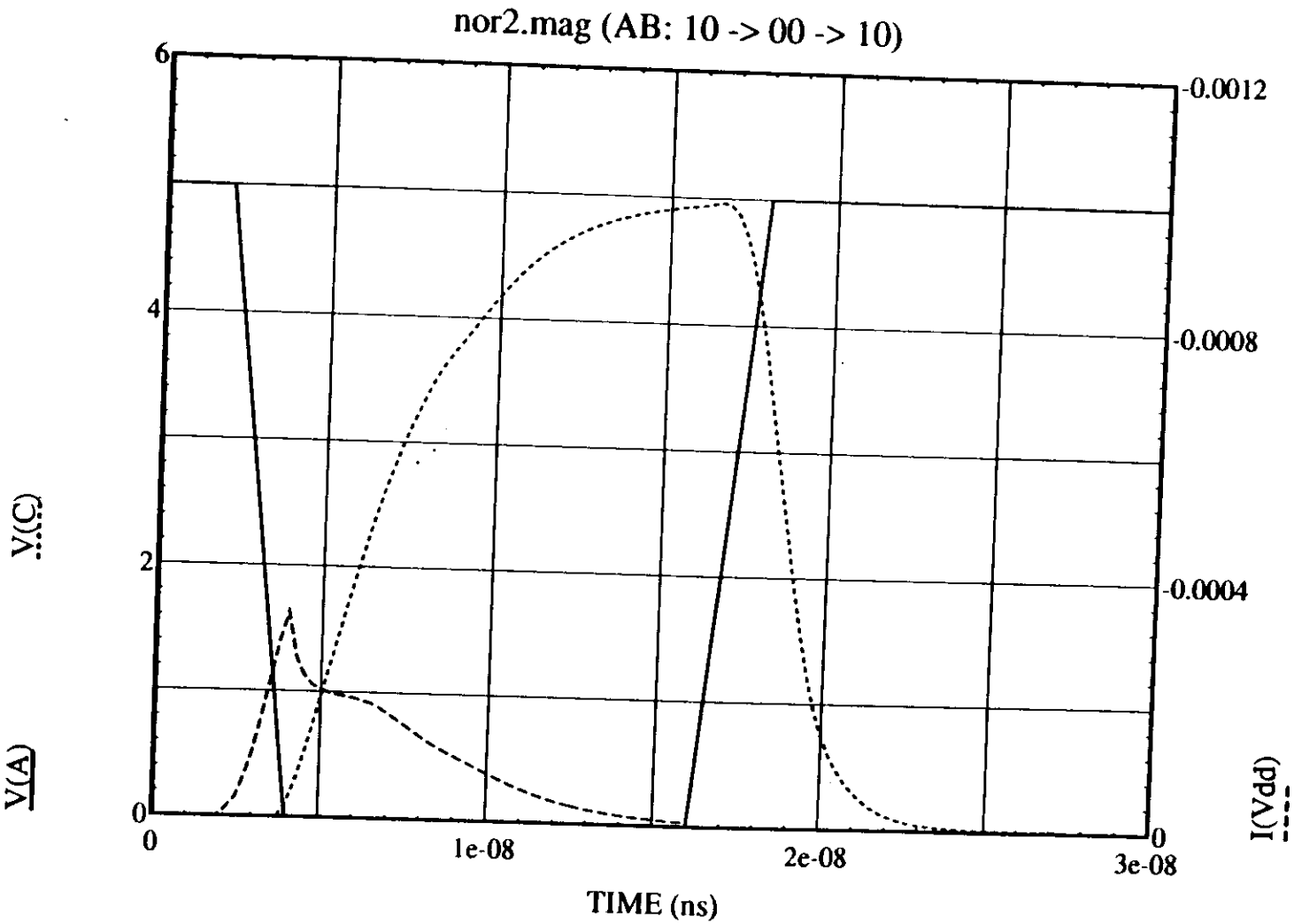

nand3.mag (ABC: 111 -> 011 -> 111)
6
4
2
0
-0.0012
-0.0008
-0.0004
0
0
1e-08
2e-08
3e-08
TIME (ns)
V(A)
V(D)
I(Vdd)

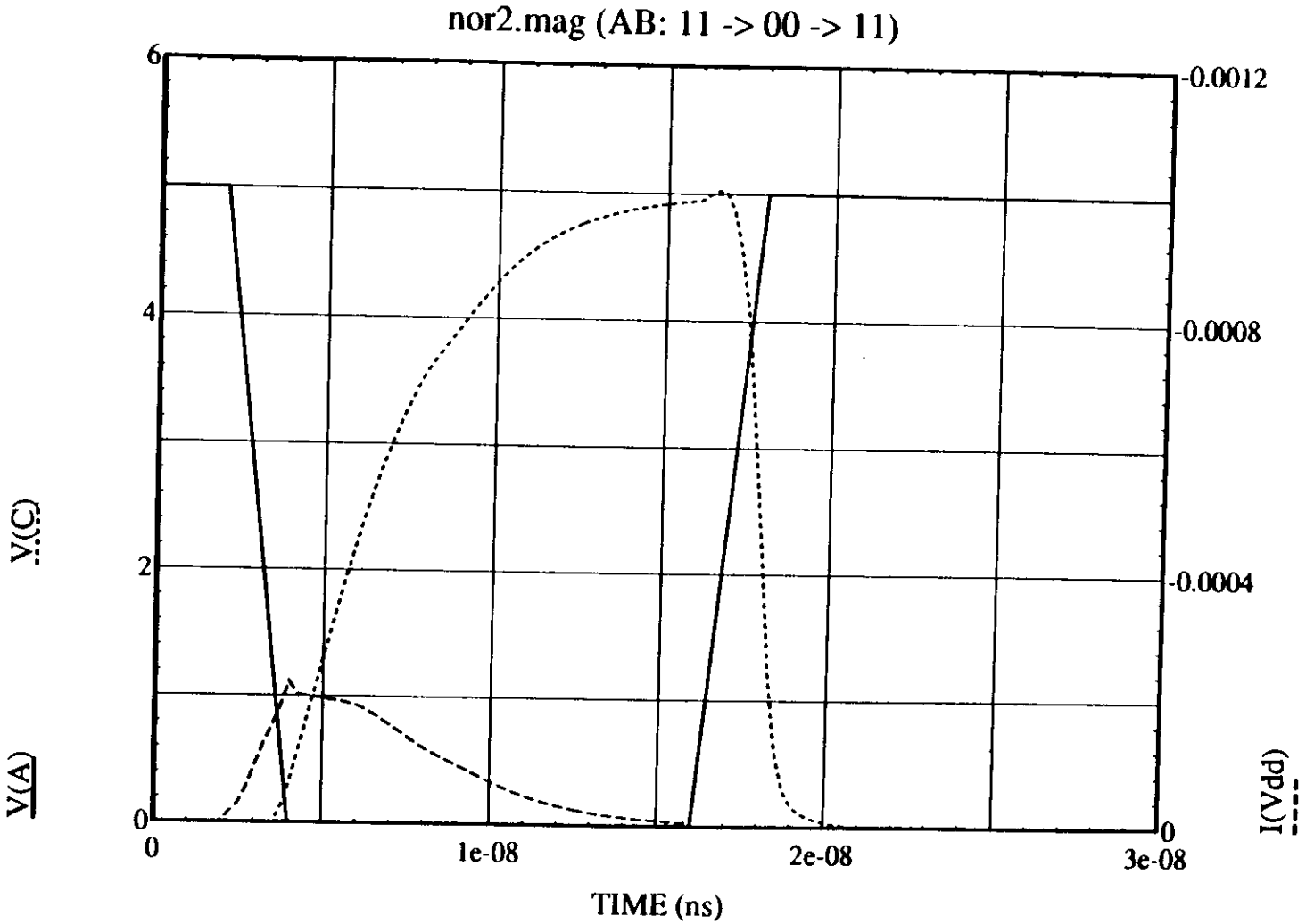
```
*  Simulation of cell:  nand3.mag (ABC: 111 -> 000 -> 111)      HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,12ns)
define(TF,2ns)
define(TL,12ns)
define(PER,28ns)
define(TIME,30ns)
*
*
*    \       A       /
*     \______________/
*
*    \       B       /
*     \______________/
*
*    \       C       /
*     \______________/
*                                                          HERE
VA  20  0  pulse(5 0 TD TR TF TH PER)
VB  21  0  pulse(5 0 TD TR TF TH PER)
VC  22  0  pulse(5 0 TD TR TF TH PER)
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*                                                          HERE
.tran 0.25ns TIME
.print trans v(20) v(23) i(Vdd)
.print trans v(100)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit input (= load)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
*                                                          HERE
XLOAD 2 4 5 23 100 load
*
include(/icsl2/dloh/spice.dir/load)
*
include(/icsl2/dloh/spice.dir/power)
*                                                          HERE
include(/icsl2/dloh/spice.dir/nand3.dir/nand3.spice)
*
include(/icsl2/dloh/spice.dir/models)
*
.end
```


nand3.mag (ABC: 111 -> 000 -> 111)
6
4
2
0
-0.0012
-0.0008
-0.0004
0
0
1e-08
2e-08
3e-08
TIME (ns)
V(A)
V(D)
I(Vdd)

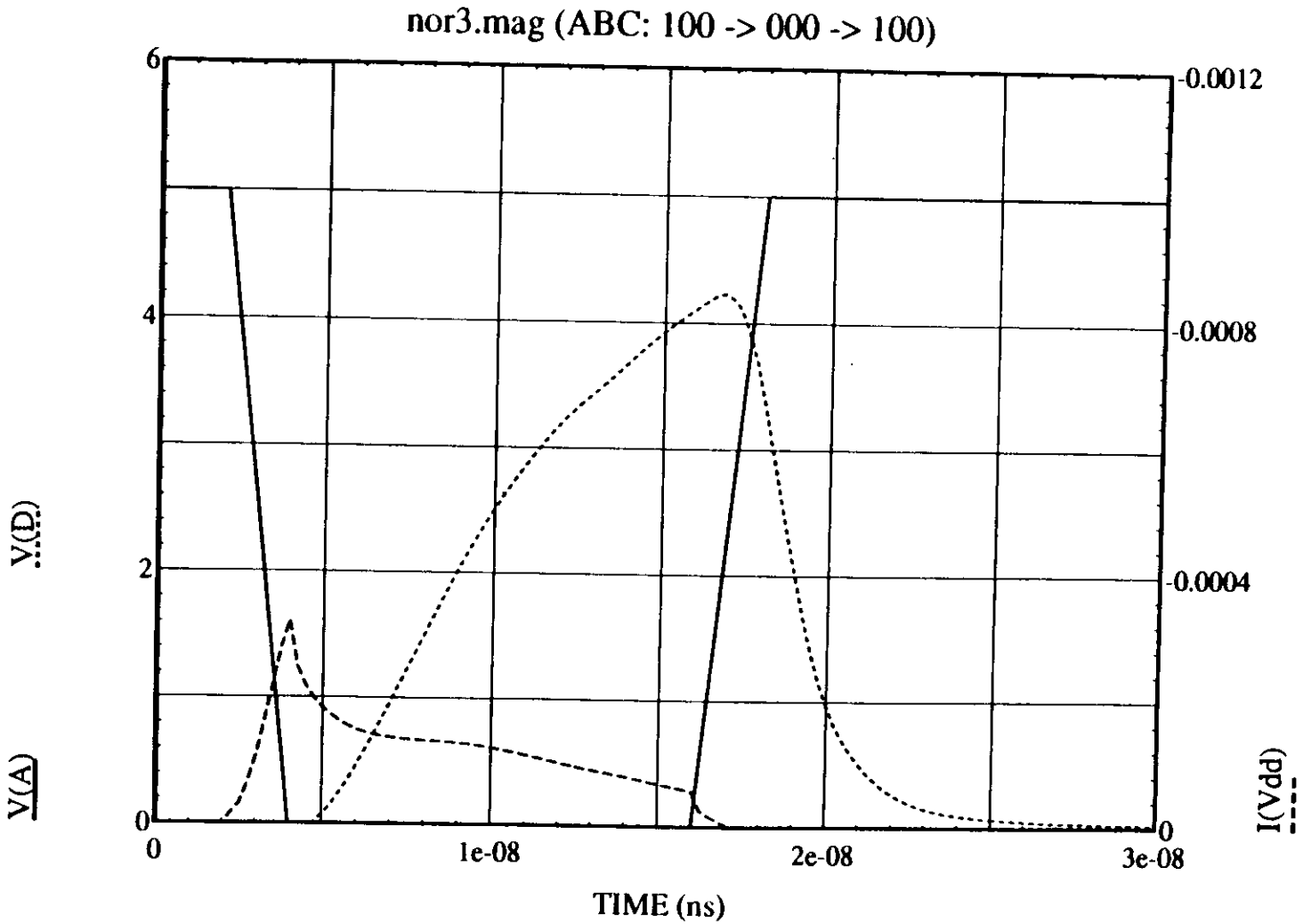
```
*  Simulation of cell:  nor2.mag (AB: 10 -> 00 -> 10)      HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,12ns)
define(TF,2ns)
define(TL,12ns)
define(PER,28ns)
define(TIME,30ns)
*
*
*___      A       ___________
*   \              /
*    \____________/
*
VA  20  0  pulse(5 0 TD TR TF TH PER)                    HERE
VB  21  0  0V
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*
.tran 0.25ns TIME                                        HERE
.print trans v(20) v(22) i(Vdd)
.print trans v(100)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit input (= load)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
*
XLOAD 2 4 5 22 100 load                                  HERE
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*
include(/ics12/dloh/spice.dir/nor2.dir/nor2.spice)       HERE
*
include(/ics12/dloh/spice.dir/models)
*
.end
```

```
*  Simulation of cell:  nor2.mag (AB: 11 -> 00 -> 11)        HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,12ns)
define(TF,2ns)
define(TL,12ns)
define(PER,28ns)
define(TIME,30ns)
*
*
*___
*   \       A       /___________
*    \_____________/
*
*___
*   \       B       /___________
*    \_____________/
*
VA  20  0  pulse(5 0 TD TR TF TH PER)                    HERE
VB  21  0  pulse(5 0 TD TR TF TH PER)
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*
.tran 0.25ns TIME                                        HERE
.print trans v(20) v(22) i(Vdd)
.print trans v(100)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit input (= load)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
*
XLOAD 2 4 5 22 100 load                                  HERE
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*
include(/ics12/dloh/spice.dir/nor2.dir/nor2.spice)       HERE
*
include(/ics12/dloh/spice.dir/models)
*
.end
```

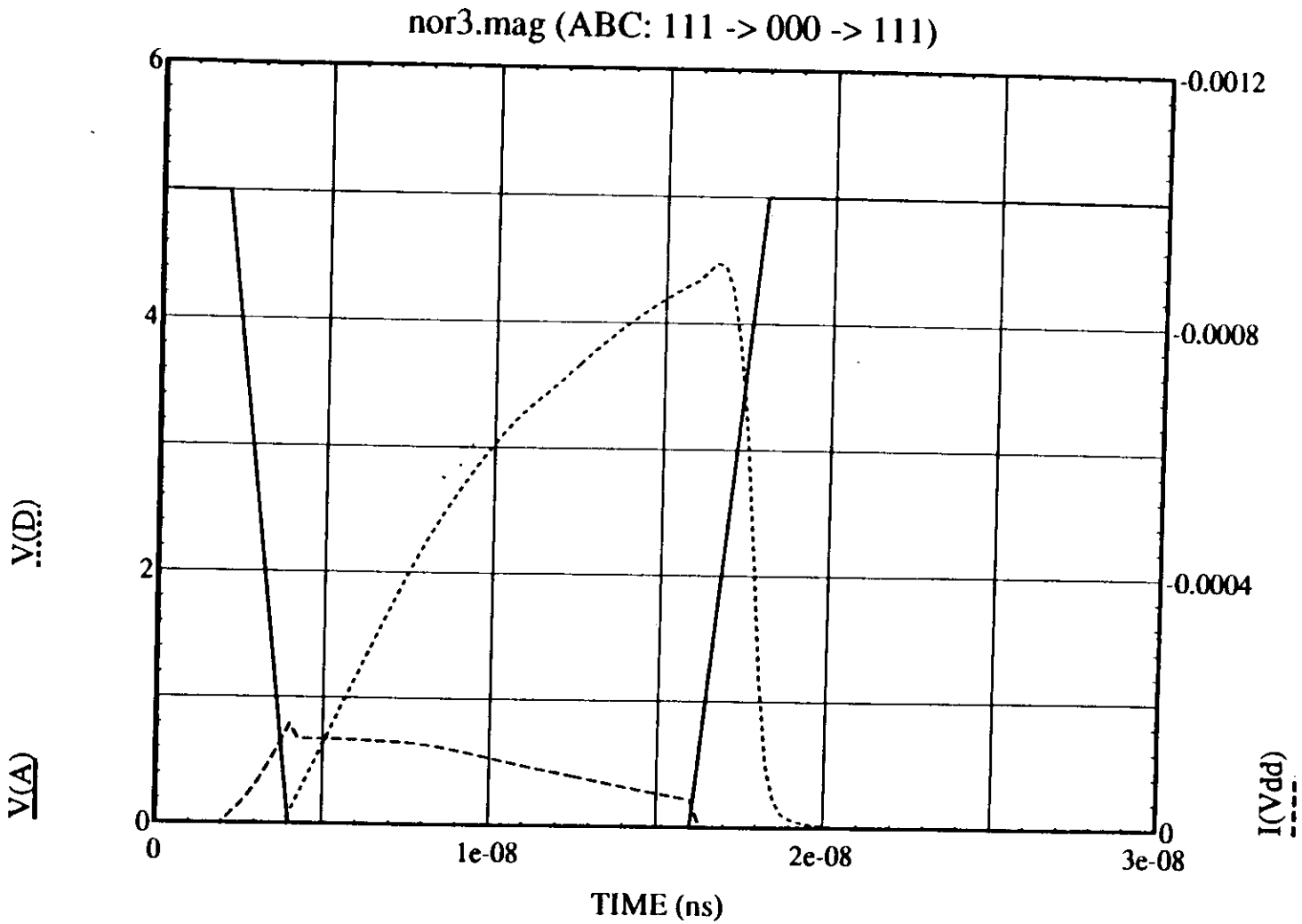

nor2.mag (AB: 10 -> 00 -> 10)
6
4
2
0
-0.0012
-0.0008
-0.0004
0
0
1e-08
2e-08
3e-08
TIME (ns)
V(A)
V(C)
I(Vdd)


nor2.mag (AB: 11 -> 00 -> 11)
6
4
2
0
V(A)
V(C)
-0.0012
-0.0008
-0.0004
0
I(VdD)
0
1e-08
2e-08
3e-08
TIME (ns)

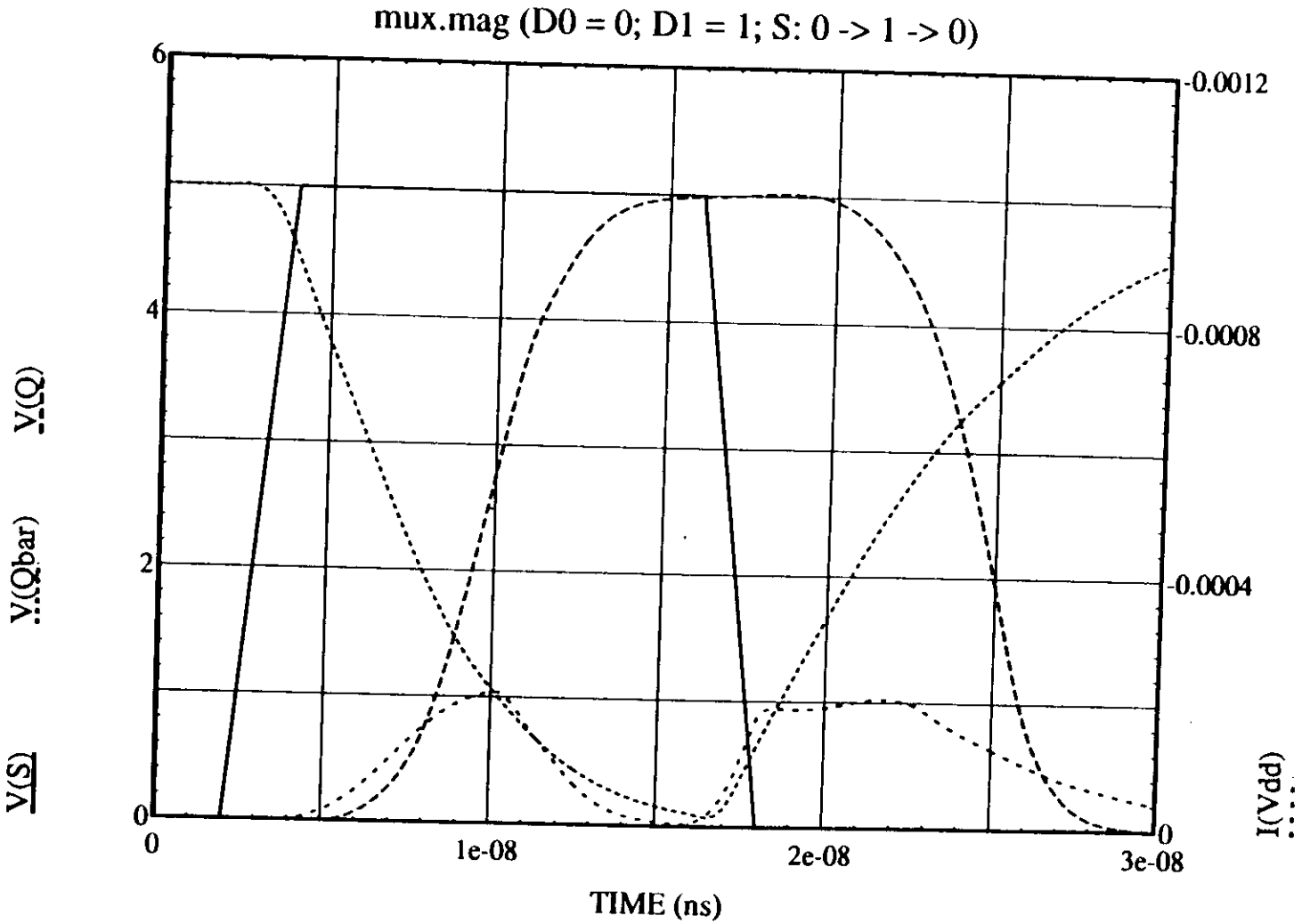
```
*  Simulation of cell:  nor3.mag (ABC: 100 -> 000 -> 100)      HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,12ns)
define(TF,2ns)
define(TL,12ns)
define(PER,28ns)
define(TIME,30ns)
*
*
*___
*    \       A       /____________
*     \_____________/
*                                                          HERE
VA   20   0   pulse(5 0 TD TR TF TH PER)
VB   21   0   0V
VC   22   0   0V
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*                                                          HERE
.tran 0.25ns TIME
.print trans v(20) v(23) i(Vdd)
.print trans v(100)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit input (= load)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
*                                                          HERE
XLOAD 2 4 5 23 100 load
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*                                                          HERE
include(/ics12/dloh/spice.dir/nor3.dir/nor3.spice)
*
include(/ics12/dloh/spice.dir/models)
*
.end
```


nor3.mag (ABC: 100 -> 000 -> 100)
6
4
2
0
-0.0012
-0.0008
-0.0004
0
0
1e-08
2e-08
3e-08
TIME (ns)
V(A)
V(D)
I(Vdd)

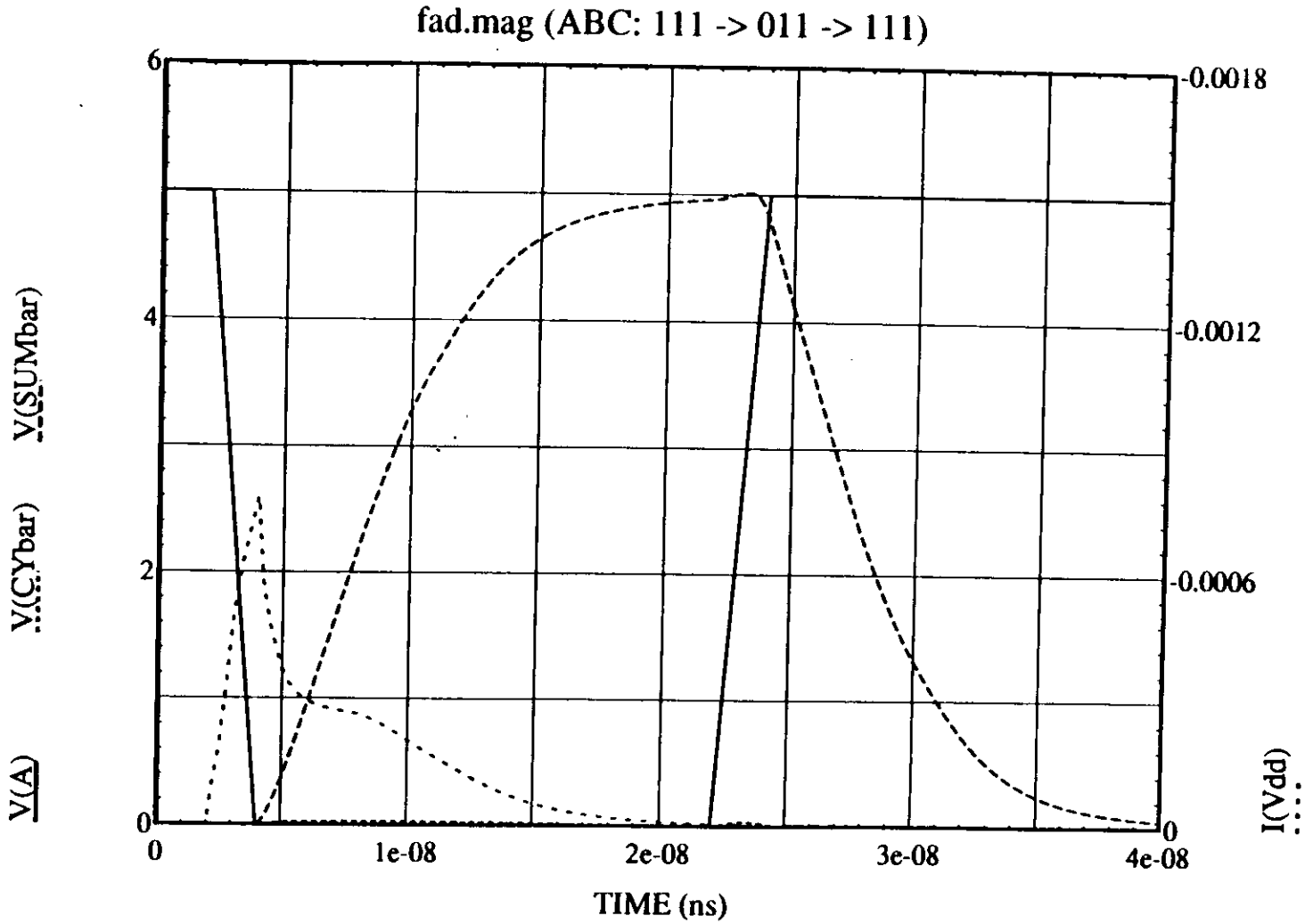
```
*  Simulation of cell:  nor3.mag (ABC: 111 -> 000 -> 111)      HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,12ns)
define(TF,2ns)
define(TL,12ns)
define(PER,28ns)
define(TIME,30ns)
*
*
*    \       A       /
*     \_____________/
*
*    \       B       /
*     \_____________/
*
*    \       C       /
*     \_____________/
*
VA  20  0  pulse(5 0 TD TR TF TH PER)                          HERE
VB  21  0  pulse(5 0 TD TR TF TH PER)
VC  22  0  pulse(5 0 TD TR TF TH PER)
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*
.tran 0.25ns TIME                                              HERE
.print trans v(20) v(23) i(Vdd)
.print trans v(100)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit input (= load)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
*
XLOAD 2 4 5 23 100 load                                        HERE
*
include(/icsl2/dloh/spice.dir/load)
*
include(/icsl2/dloh/spice.dir/power)
*                                                              HERE
include(/icsl2/dloh/spice.dir/nor3.dir/nor3.spice)
*
include(/icsl2/dloh/spice.dir/models)
*
.end
```


nor3.mag (ABC: 111 -> 000 -> 111)
6
4
2
0
-0.0012
-0.0008
-0.0004
0
0
1e-08
2e-08
3e-08
TIME (ns)
V(A)
V(D)
I(Vdd)

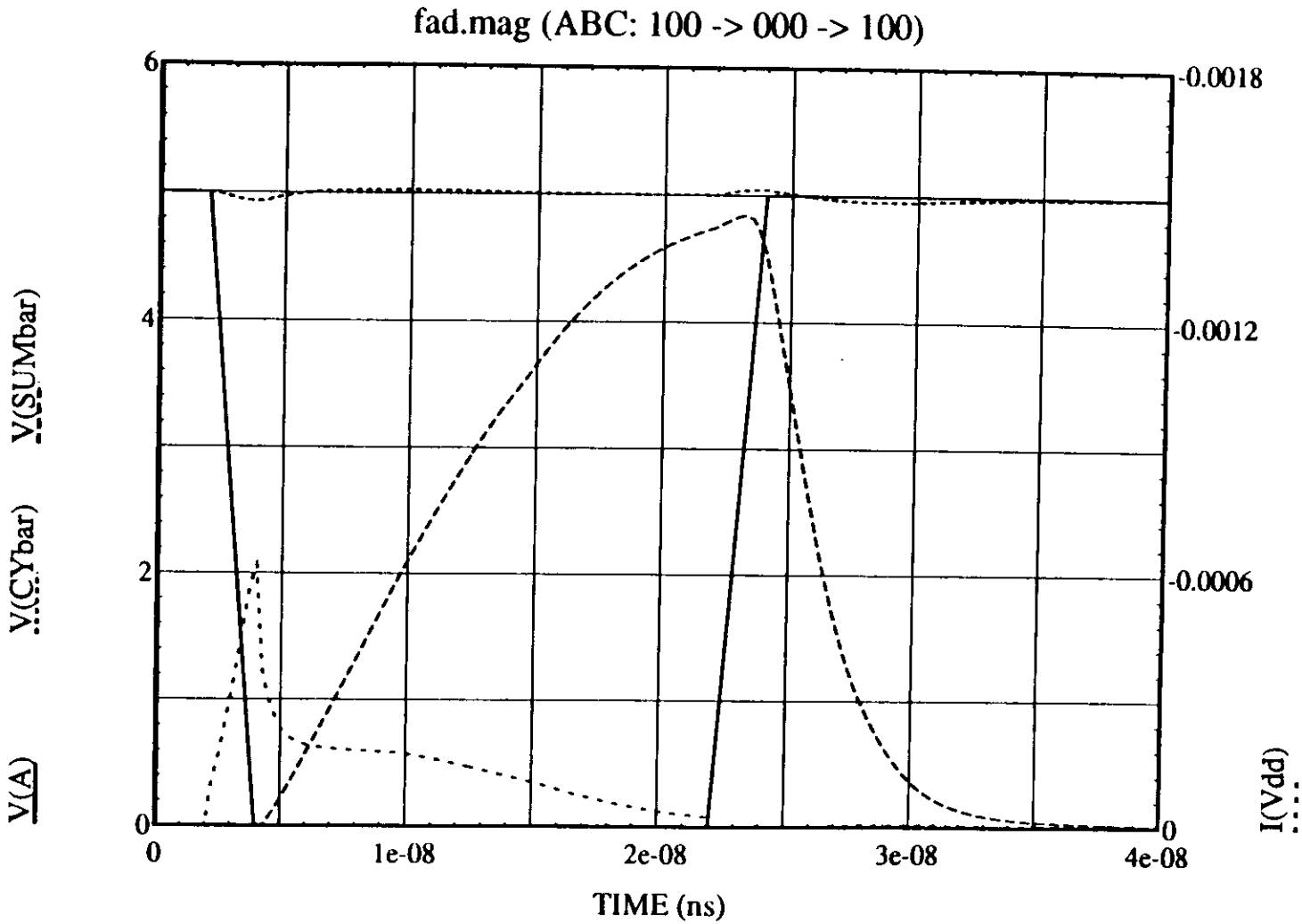
```
*  Simulation of cell:  mux.mag (D0 = 0; D1 = 1; S: 0 -> 1 -> 0)     HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,12ns)
define(TF,2ns)
define(TL,12ns)
define(PER,28ns)
define(TIME,30ns)
*
*
*     ____________
*    /            \
*___/       S      \_____________
*
*___
*    \      Sbar    /_____________
*     \____________/
*
VS      26  0  pulse(0 5 TD TR TF TH PER)                          HERE
VSbar   27  0  pulse(5 0 TD TR TF TH PER)
VD0     24  0  0V
VD1     25  0  5V
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*
.tran 0.25ns TIME                                                  HERE
.print trans v(26) v(43) v(42) i(Vdd)
.print trans v(100) v(101)
.options nomod ingold=2
.width out=80
*
*  Pass cell outputs to subcircuit input (= load)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
XLOADQbar 2 4 5 43 100 load                                        HERE
XLOADQ    2 4 5 42 101 load
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*
include(/ics12/dloh/spice.dir/mux.dir/mux.spice)                   HERE
*
include(/ics12/dloh/spice.dir/models)
*
.end
```


mux.mag (D0 = 0; D1 = 1; S: 0 -> 1 -> 0)
V(S)
V(Qbar)
V(Q)
I(Vdd)
TIME (ns)
0
2
4
6
-0.0012
-0.0008
-0.0004
0
1e-08
2e-08
3e-08

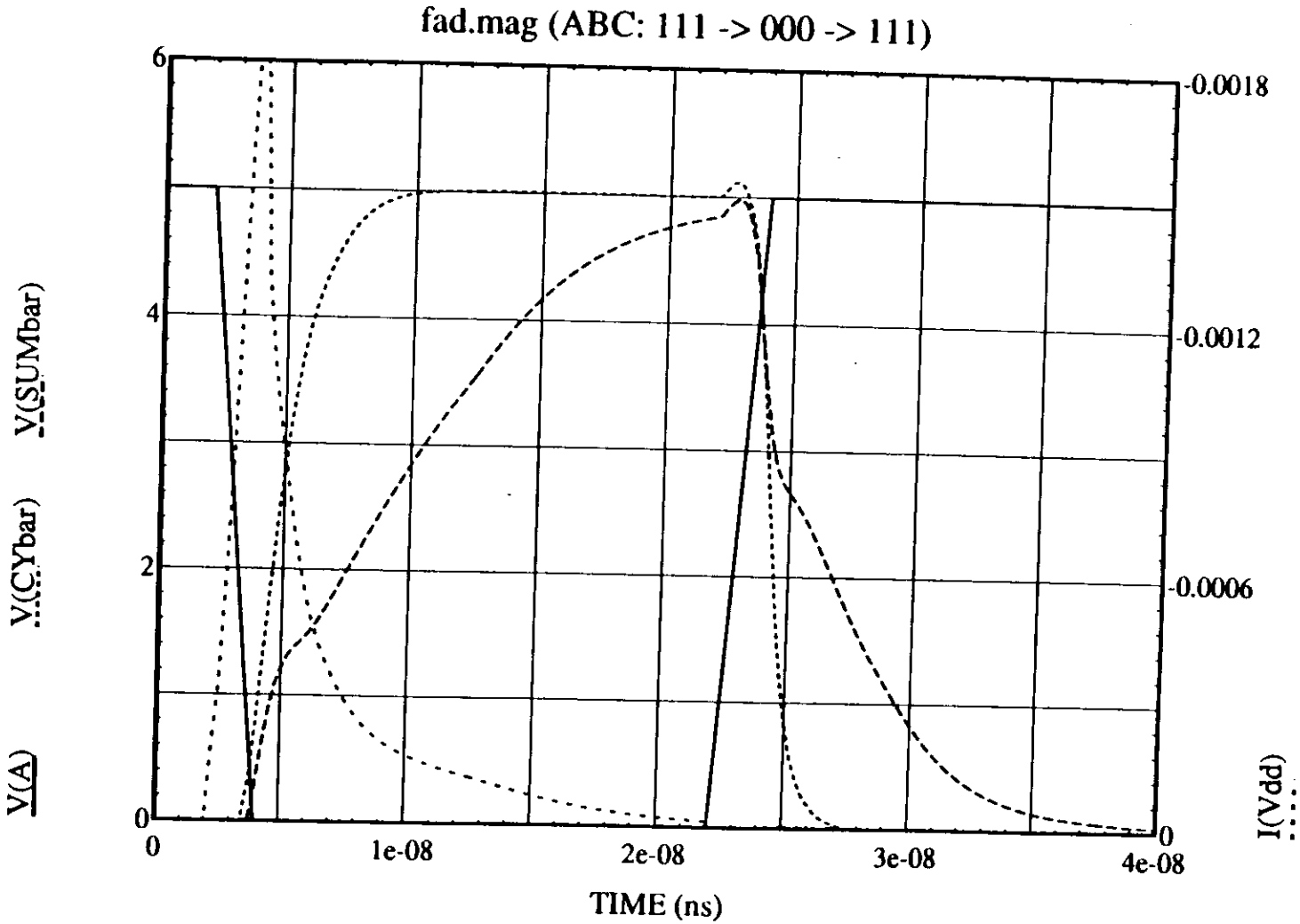
```
*  Simulation of cell:  fad.mag (ABC: 111 -> 011 -> 111)      HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,18ns)
define(TF,2ns)
define(TL,18ns)
define(PER,40ns)
define(TIME,42ns)
*
*
*___
*   \       A       /____________
*    \______________/
*                                                          HERE
VA  20  0  pulse(5 0 TD TR TF TH PER)
VB  21  0  5V
VC  22  0  5V
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*                                                          HERE
.tran 0.25ns TIME
.print trans v(20) v(40) v(41) i(Vdd)
.print trans v(100) v(101)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit inputs (= loads)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
*                                                          HERE
XCYbar  2 4 5 40 100 load
XSUMbar 2 4 5 41 101 load
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*                                                          HERE
include(/ics12/dloh/spice.dir/fad.dir/fad.spice)
*
include(/ics12/dloh/spice.dir/models)
*
.end
```


fad.mag (ABC: 111 -> 011 -> 111)
V(A)
V(CYbar)
V(SUMbar)
I(Vdd)
6
4
2
0
-0.0018
-0.0012
-0.0006
0
0
1e-08
2e-08
3e-08
4e-08
TIME (ns)

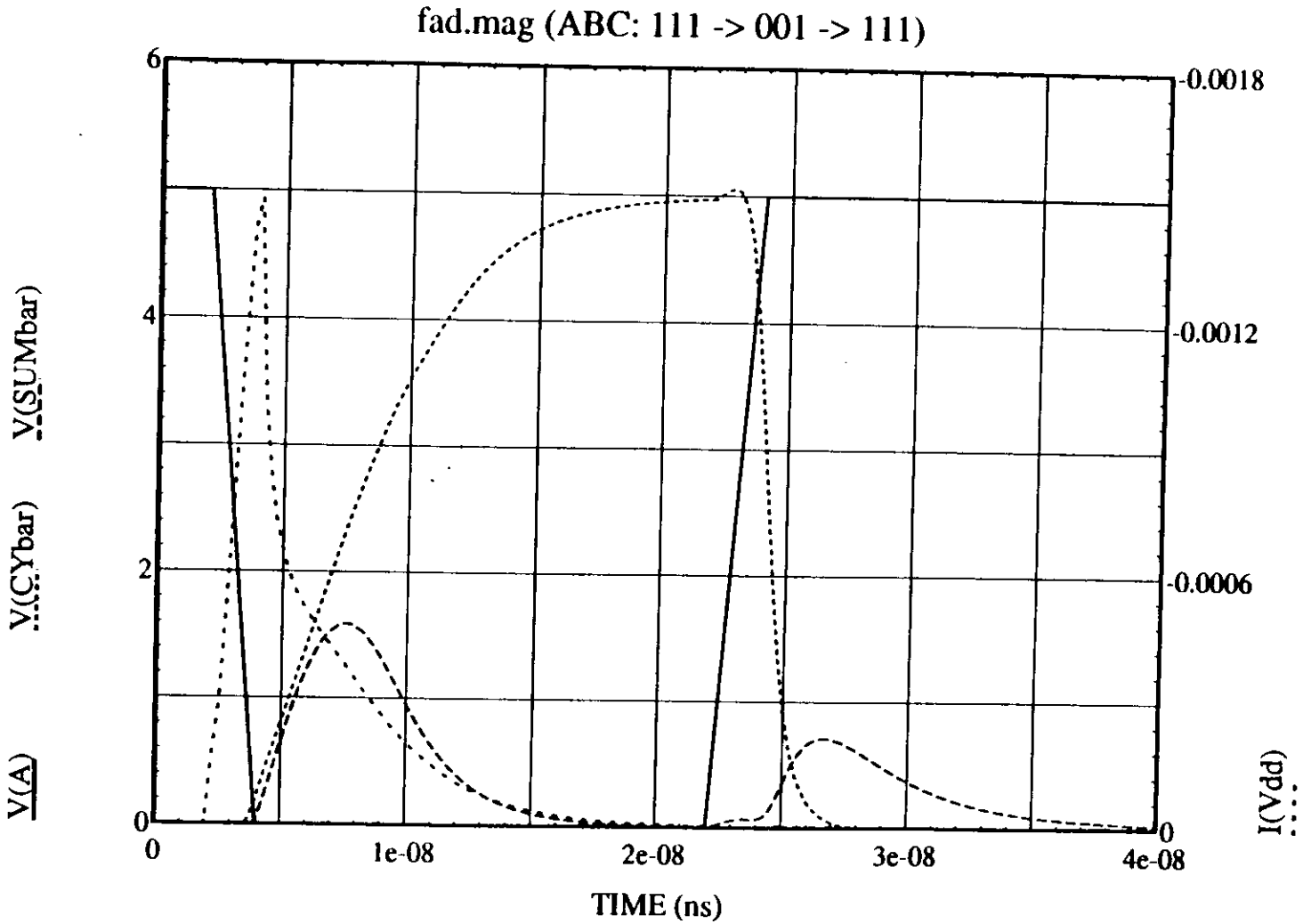
```
*  Simulation of cell:  fad.mag (ABC: 100 -> 000 -> 100)      HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,18ns)
define(TF,2ns)
define(TL,18ns)
define(PER,40ns)
define(TIME,42ns)
*
*
*___      \       A       /____________
*    \_____________/
*
VA  20  0  pulse(5 0 TD TR TF TH PER)                          HERE
VB  21  0  0V
VC  22  0  0V
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*
.tran 0.25ns TIME                                              HERE
.print trans v(20) v(40) v(41) i(Vdd)
.print trans v(100) v(101)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit inputs (= loads)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
*
XCYbar  2 4 5 40 100 load                                      HERE
XSUMbar 2 4 5 41 101 load
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*
include(/ics12/dloh/spice.dir/fad.dir/fad.spice)               HERE
*
include(/ics12/dloh/spice.dir/models)
*
.end
```


fad.mag (ABC: 100 -> 000 -> 100)
V(A)
V(CYbar)
V(SUMbar)
I(Vdd)
6
4
2
0
-0.0018
-0.0012
-0.0006
0
0
1e-08
2e-08
3e-08
4e-08
TIME (ns)

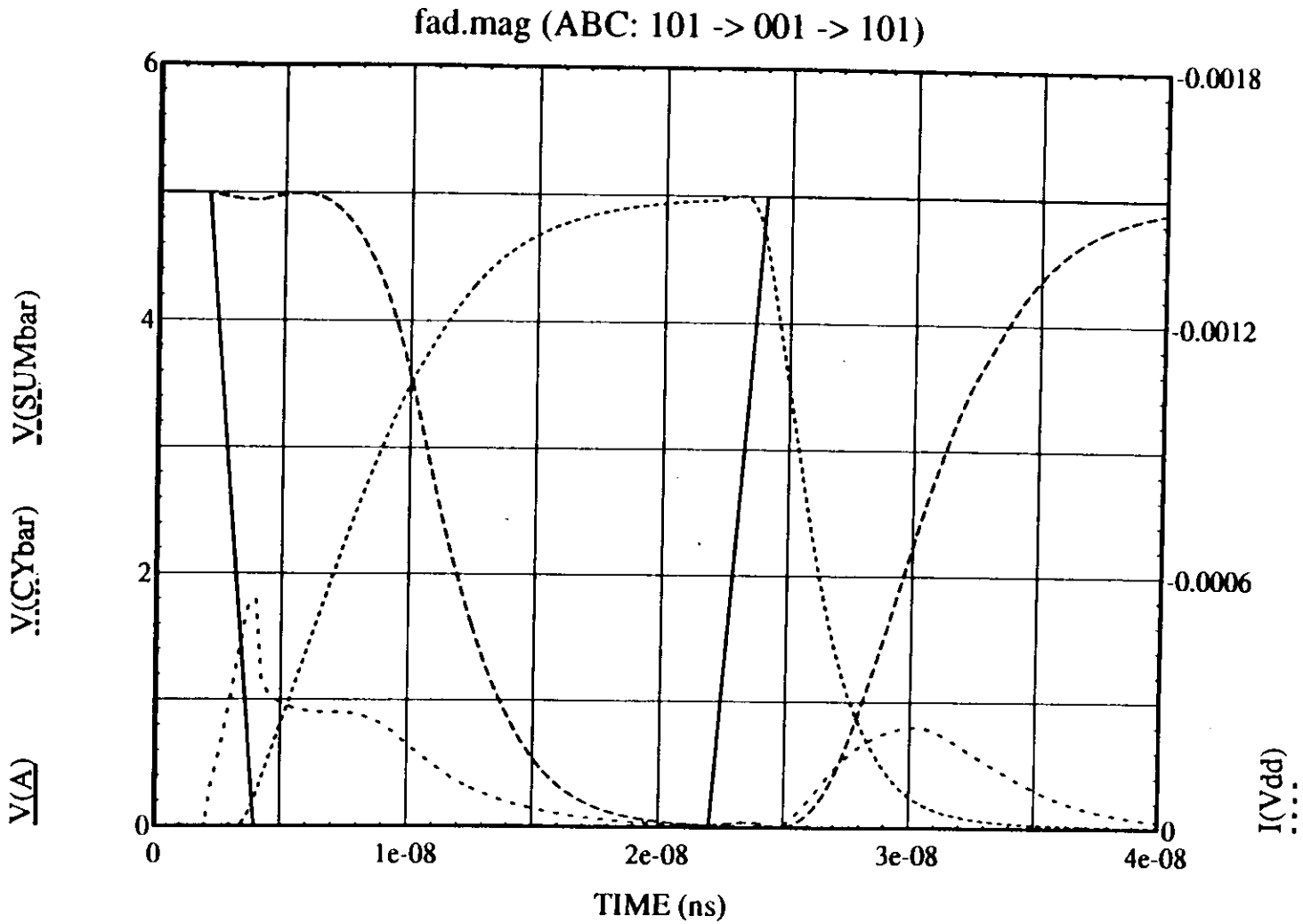
```
*  Simulation of cell:  fad.mag (ABC: 111 -> 000 -> 111)        HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,18ns)
define(TF,2ns)
define(TL,18ns)
define(PER,40ns)
define(TIME,42ns)
*
*
*___    \       A       /____________
*    \_____________/
*
*___    \       B       /____________
*    \_____________/
*
*___    \       C       /____________
*    \_____________/
*
VA  20  0  pulse(5 0 TD TR TF TH PER)                        HERE
VB  21  0  pulse(5 0 TD TR TF TH PER)
VC  22  0  pulse(5 0 TD TR TF TH PER)
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respec.ively
*
*
.tran 0.25ns TIME                                            HERE
.print trans v(20) v(40) v(41) i(Vdd)
.print trans v(100) v(101)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit inputs (= loads)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
*
XCYbar  2 4 5 40 100 load                                    HERE
XSUMbar 2 4 5 41 101 load
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*
include(/ics12/dloh/spice.dir/fad.dir/fad.spice)             HERE
*
include(/ics12/dloh/spice.dir/models)
*
.end
```


fad.mag (ABC: 111 -> 000 -> 111)
V(A)
V(CYbar)
V(SUMbar)
I(Vdd)
6
4
2
0
-0.0018
-0.0012
-0.0006
0
0
1e-08
2e-08
3e-08
4e-08
TIME (ns)

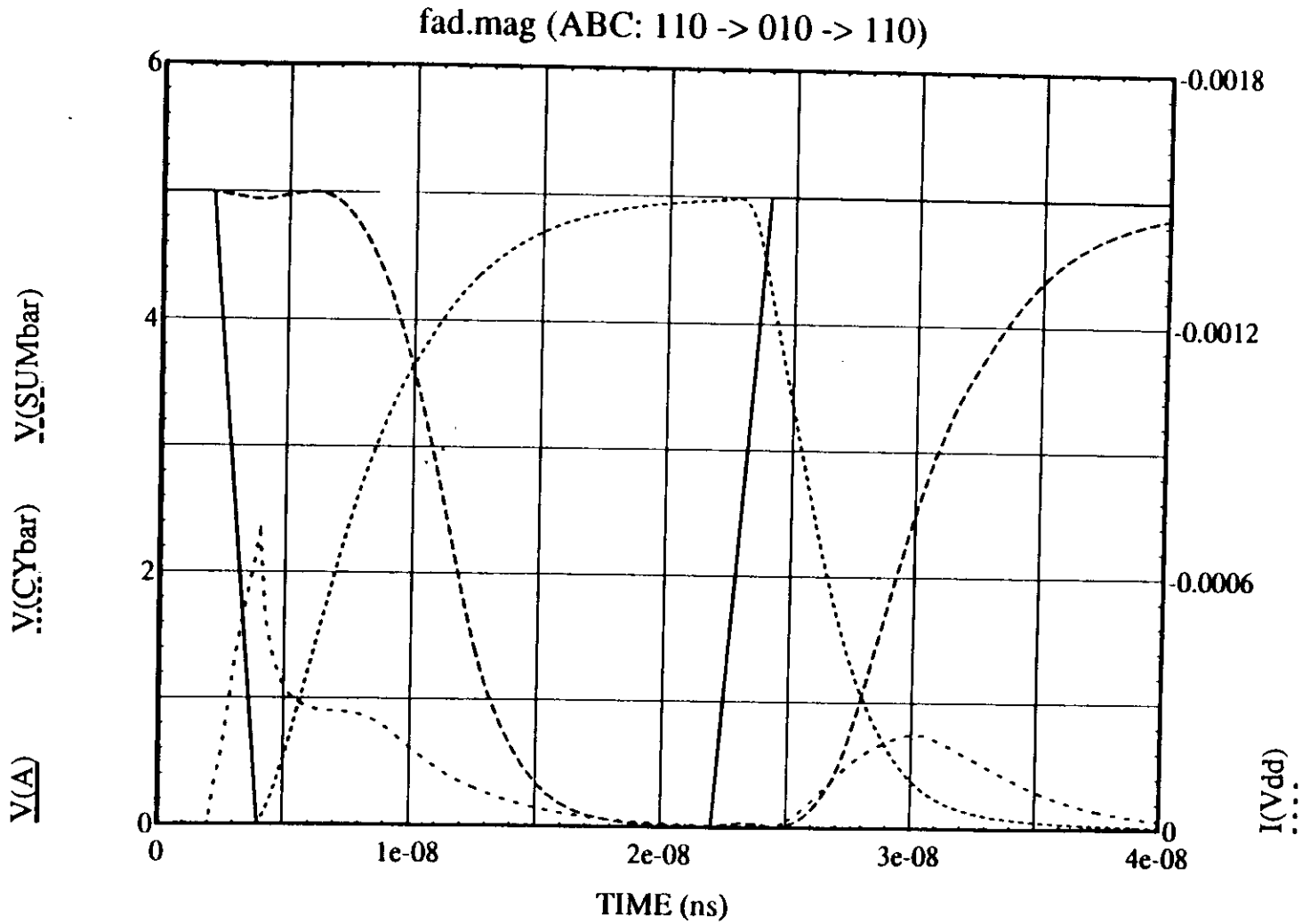
```
*  Simulation of cell:  fad.mag (ABC: 101 -> 001 -> 101)      HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,18ns)
define(TF,2ns)
define(TL,18ns)
define(PER,40ns)
define(TIME,42ns)
*
*
*    \       A       /
*     \______________/
*
VA  20  0  pulse(5 0 TD TR TF TH PER)                          HERE
VB  21  0  0V
VC  22  0  5V
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*
.tran 0.25ns TIME                                              HERE
.print trans v(20) v(40) v(41) i(Vdd)
.print trans v(100) v(101)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit inputs (= loads)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
*
XCYbar  2 4 5 40 100 load                                      HERE
XSUMbar 2 4 5 41 101 load
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*
include(/ics12/dloh/spice.dir/fad.dir/fad.spice)               HERE
*
include(/ics12/dloh/spice.dir/models)
*
.end
```


fad.mag (ABC: 111 -> 001 -> 111)
V(A)
V(CYbar)
V(SUMbar)
I(Vdd)
6
4
2
0
-0.0018
-0.0012
-0.0006
0
0
1e-08
2e-08
3e-08
4e-08
TIME (ns)

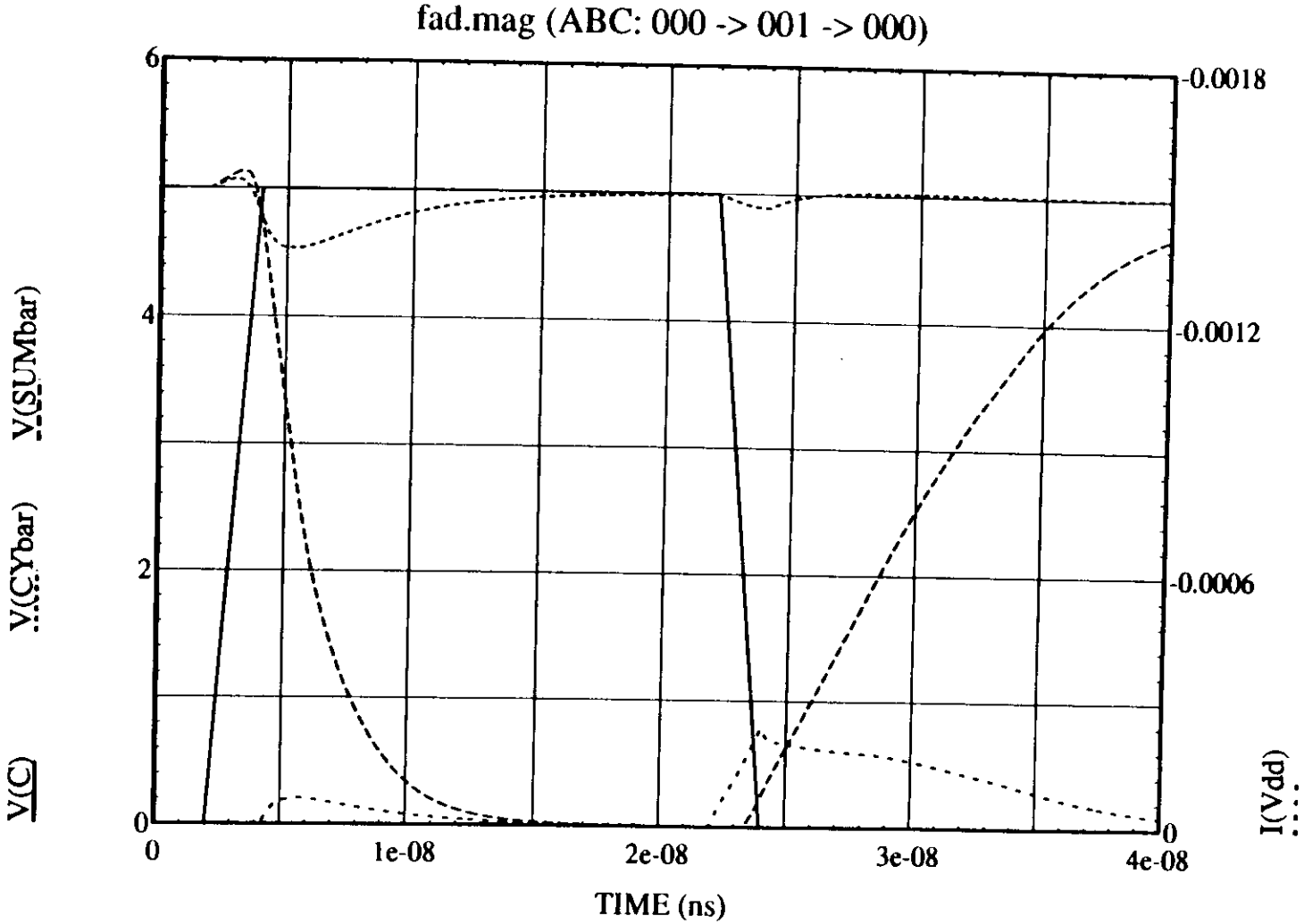
```
*  Simulation of cell:  fad.mag (ABC: 110 -> 010 -> 110)      HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,18ns)
define(TF,2ns)
define(TL,18ns)
define(PER,40ns)
define(TIME,42ns)
*
*
*___
*   \       A        /____________
*    \_______________/
*                                                          HERE
VA  20  0  pulse(5 0 TD TR TF TH PER)
VB  21  0  5V
VC  22  0  0V
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*                                                          HERE
.tran 0.25ns TIME
.print trans v(20) v(40) v(41) i(Vdd)
.print trans v(100) v(101)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit inputs (= loads)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
*                                                          HERE
XCYbar  2 4 5 40 100 load
XSUMbar 2 4 5 41 101 load
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*                                                          HERE
include(/ics12/dloh/spice.dir/fad.dir/fad.spice)
*
include(/ics12/dloh/spice.dir/models)
*
.end
```


fad.mag (ABC: 101 -> 001 -> 101)
V(A)
V(CYbar)
V(SUMbar)
I(Vdd)
6
4
2
0
-0.0018
-0.0012
-0.0006
0
0
1e-08
2e-08
3e-08
4e-08
TIME (ns)

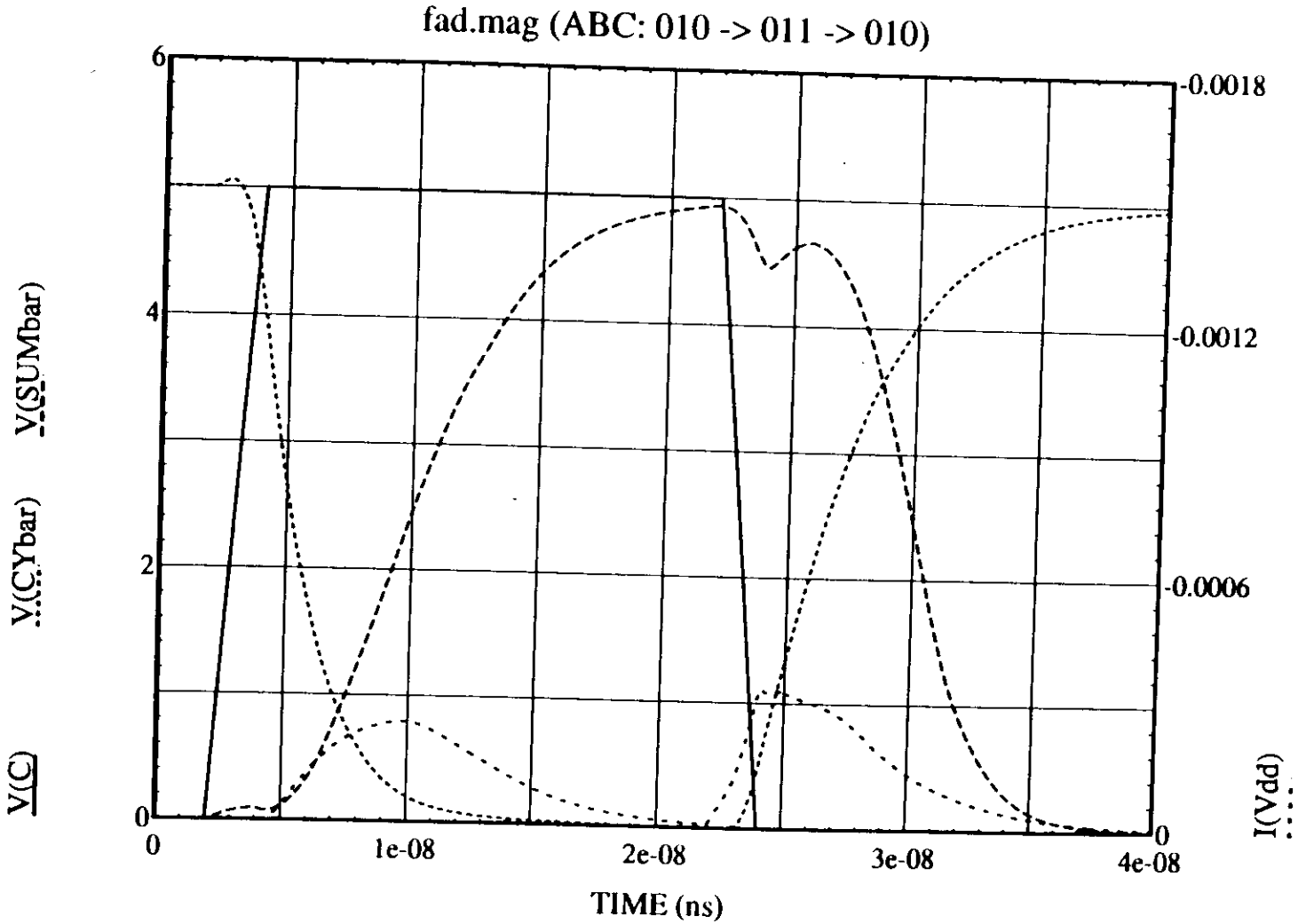
```
*  Simulation of cell:  fad.mag (ABC: 000 -> 001 -> 000)      HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,18ns)
define(TF,2ns)
define(TL,18ns)
define(PER,40ns)
define(TIME,42ns)
*
*
*     ____________
*    /            \
*___/       C      \___________
*
VA  20  0  0V                                                  HERE
VB  21  0  0V
VC  22  0  pulse(0 5 TD TR TF TH PER)
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*
.tran 0.25ns TIME                                              HERE
.print trans v(22) v(40) v(41) i(Vdd)
.print trans v(100) v(101)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit inputs (= loads)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
*
XCYbar  2 4 5 40 100 load                                      HERE
XSUMbar 2 4 5 41 101 load
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*
include(/ics12/dloh/spice.dir/fad.dir/fad.spice)               HERE
*
include(/ics12/dloh/spice.dir/models)
*
.end
```


fad.mag (ABC: 110 -> 010 -> 110)
V(A)
V(CYbar)
V(SUMbar)
I(Vdd)
6
4
2
0
-0.0018
-0.0012
-0.0006
0
0
1e-08
2e-08
3e-08
4e-08
TIME (ns)

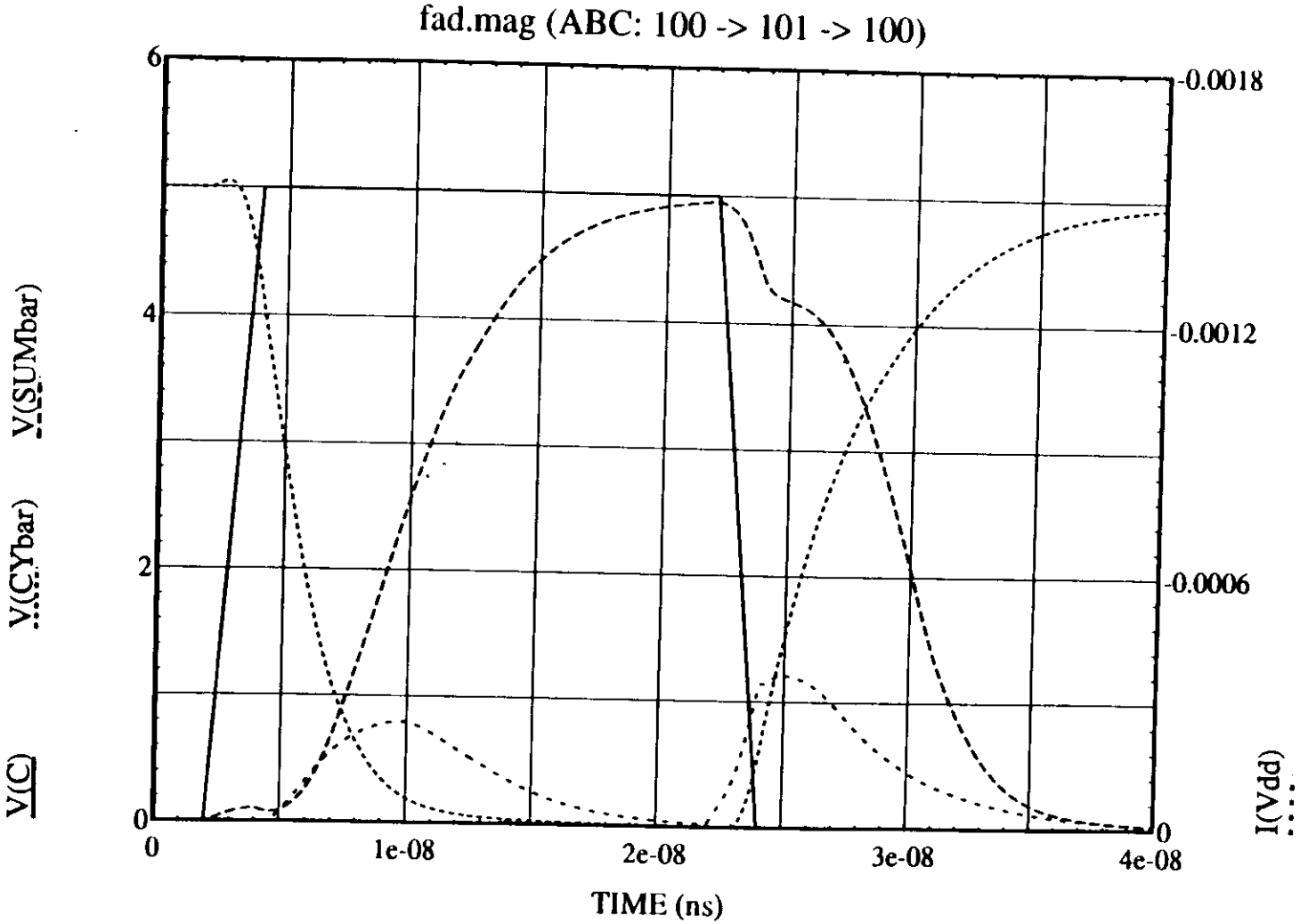
```
*  Simulation of cell:  fad.mag (ABC: 010 -> 011 -> 010)      HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,18ns)
define(TF,2ns)
define(TL,18ns)
define(PER,40ns)
define(TIME,42ns)
*
*
*      ____________
*     /            \
*____/       C      \_____________
*
                                                          HERE
VA  20  0  0V
VB  21  0  5V
VC  22  0  pulse(0 5 TD TR TF TH PER)
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*
                                                          HERE
.tran 0.25ns TIME
.print trans v(22) v(40) v(41) i(Vdd)
.print trans v(100) v(101)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit inputs (= loads)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
*
                                                          HERE
XCYbar  2 4 5 40 100 load
XSUMbar 2 4 5 41 101 load
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*
                                                          HERE
include(/ics12/dloh/spice.dir/fad.dir/fad.spice)
*
include(/ics12/dloh/spice.dir/models)
*
.end
```

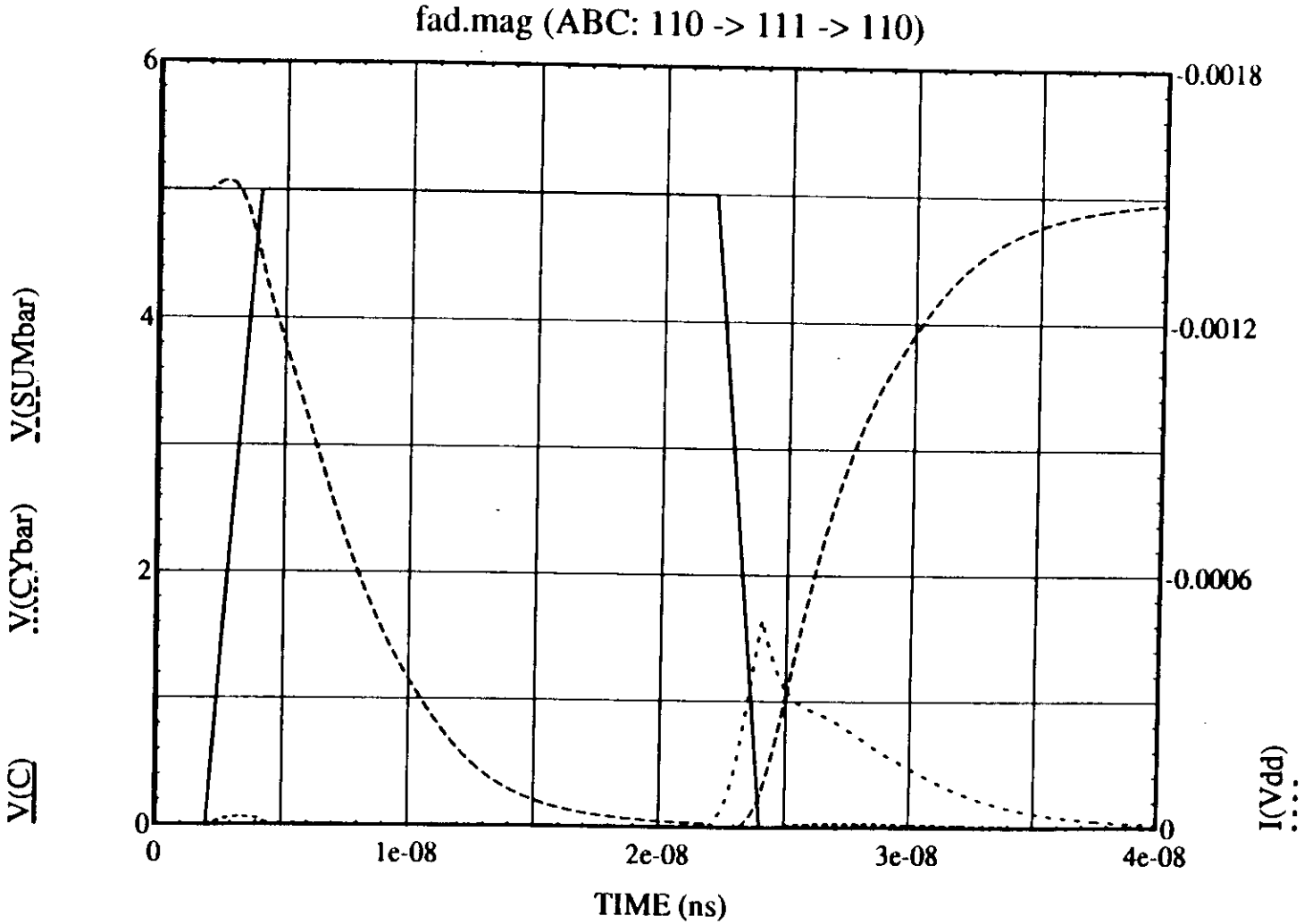

fad.mag (ABC: 000 -> 001 -> 000)
6
4
2
0
-0.0018
-0.0012
-0.0006
0
0
1e-08
2e-08
3e-08
4e-08
TIME (ns)
V(C)
V(CYbar)
V(SUMbar)
I(Vdd)

```
*  Simulation of cell:  fad.mag (ABC: 100 -> 101 -> 100)      HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,18ns)
define(TF,2ns)
define(TL,18ns)
define(PER,40ns)
define(TIME,42ns)
*
*
*     ____________
*    /            \
*___/       C      \_____________
*
VA  20  0  5V                                                  HERE
VB  21  0  0V
VC  22  0  pulse(0 5 TD TR TF TH PER)
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*
.tran 0.25ns TIME                                              HERE
.print trans v(22) v(40) v(41) i(Vdd)
.print trans v(100) v(101)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit inputs (= loads)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
*
XCYbar  2 4 5 40 100 load                                      HERE
XSUMbar 2 4 5 41 101 load
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*
include(/ics12/dloh/spice.dir/fad.dir/fad.spice)               HERE
*
include(/ics12/dloh/spice.dir/models)
*
.end
```

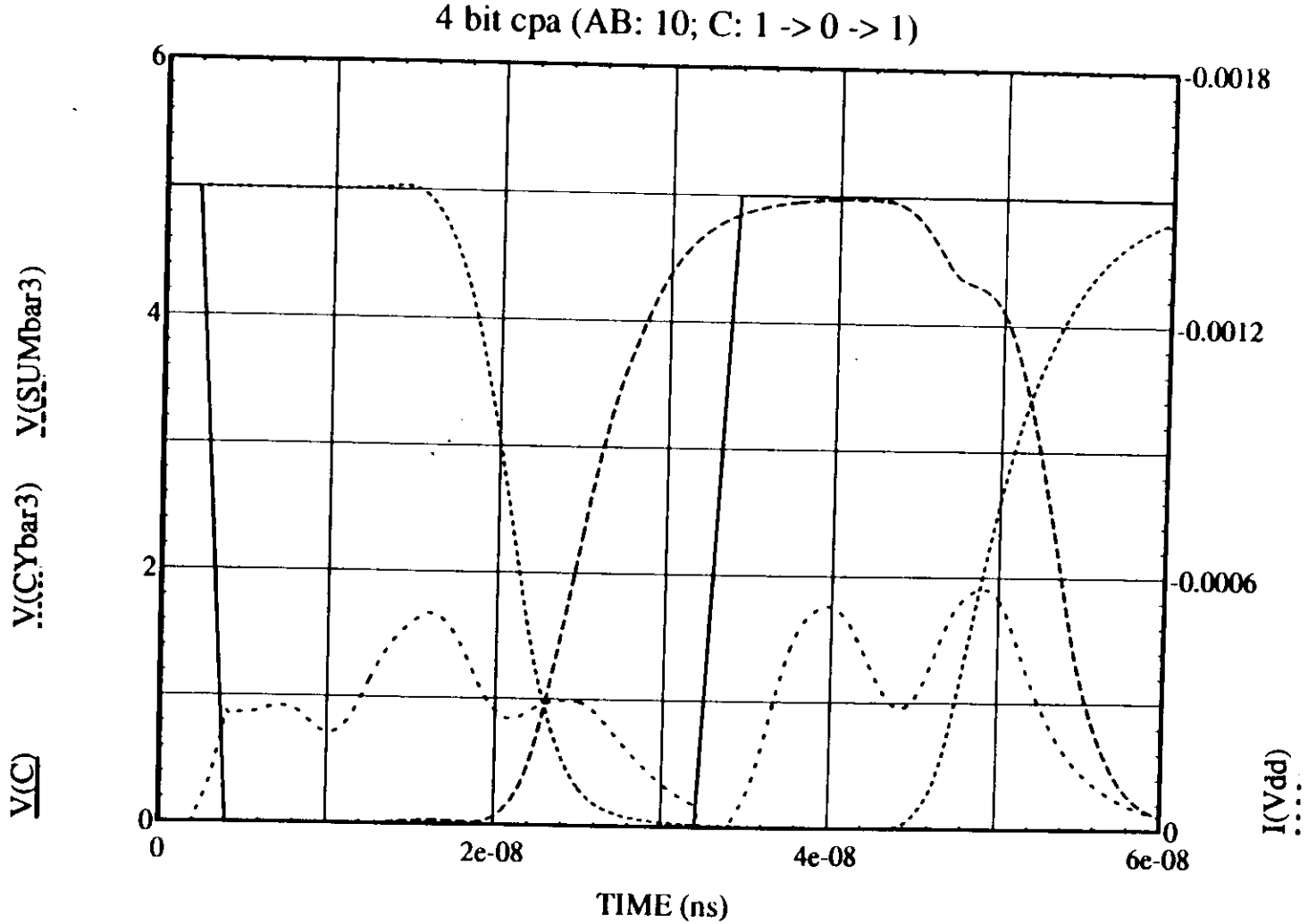

fad.mag (ABC: 010 -> 011 -> 010)
V(C)
V(CYbar)
V(SUMbar)
I(Vdd)
6
4
2
0
-0.0018
-0.0012
-0.0006
0
0
1e-08
2e-08
3e-08
4e-08
TIME (ns)

```
*  Simulation of cell:  fad.mag (ABC: 110 -> 111 -> 110)      HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,18ns)
define(TF,2ns)
define(TL,18ns)
define(PER,40ns)
define(TIME,42ns)
*
*
*     ____________
*    /            \
*___/      C       \___________
*                                                          HERE
VA  20  0  5V
VB  21  0  5V
VC  22  0  pulse(0 5 TD TR TF TH PER)
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*                                                          HERE
.tran 0.25ns TIME
.print trans v(22) v(40) v(41) i(Vdd)
.print trans v(100) v(101)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit inputs (= loads)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
*                                                          HERE
XCYbar  2 4 5 40 100 load
XSUMbar 2 4 5 41 101 load
*
include(/icsl2/dloh/spice.dir/load)
*
include(/icsl2/dloh/spice.dir/power)
*                                                          HERE
include(/icsl2/dloh/spice.dir/fad.dir/fad.spice)
*
include(/icsl2/dloh/spice.dir/models)
*
.end
```

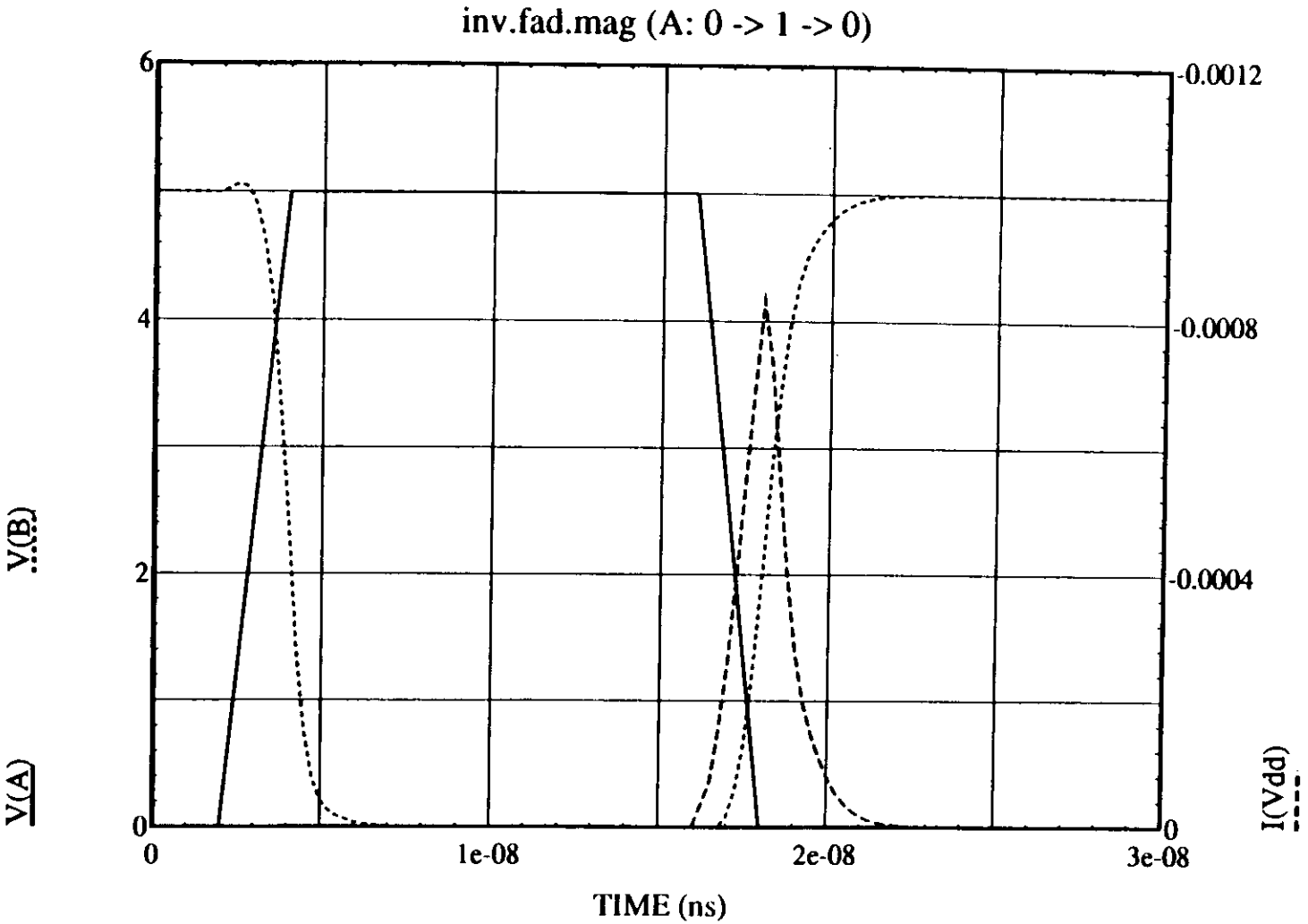

fad.mag (ABC: 100 -> 101 -> 100)
V(C)
V(CYbar)
V(SUMbar)
I(Vdd)
6
4
2
0
-0.0018
-0.0012
-0.0006
0
0
1e-08
2e-08
3e-08
4e-08
TIME (ns)


fad.mag (ABC: 110 -> 111 -> 110)
V(C)
V(CYbar)
V(SUMbar)
I(Vdd)
6
4
2
0
-0.0018
-0.0012
-0.0006
0
0
1e-08
2e-08
3e-08
4e-08
TIME (ns)

```
*  Simulation of cell:  cpa (AB = 10; C = 1 -> 0 -> 1)                HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,28ns)
define(TF,2ns)
define(TL,28ns)
define(PER,60ns)
define(TIME,62ns)
*
*
*___
*   \       C        /____________
*    \_______________/
*
VA  20  0  5V                                                      HERE
VB  21  0  0V
VC  22  0  pulse(5 0 TD TR TF TH PER)
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*
.tran 0.25ns TIME                                                  HERE
.print trans v(22) v(80) v(81) i(Vdd)
.print trans v(100) v(101)
.options nomod ingold=2
.width out=80
*
*
* FAD SUBCKT: Vdd Vcmosp Vcmosn A B C CYbar SUMbar                  HERE
*
Xfad0         1 4 5 20 21 22 50 51 fad
Xfad1         1 4 5 20 21 50 60 61 fad
Xfad2         1 4 5 20 21 60 70 71 fad
Xfad3         1 4 5 20 21 70 80 81 fad
*
*  Pass cell output to subcircuit inputs (= loads)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
XCYbar  2 4 5 80 100 load
XSUMbar 2 4 5 81 101 load
*
include(/ics12/dloh/spice.dir/cpa.dir/fad)
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*                                                                  HERE
include(/ics12/dloh/spice.dir/models)
*
.end
```

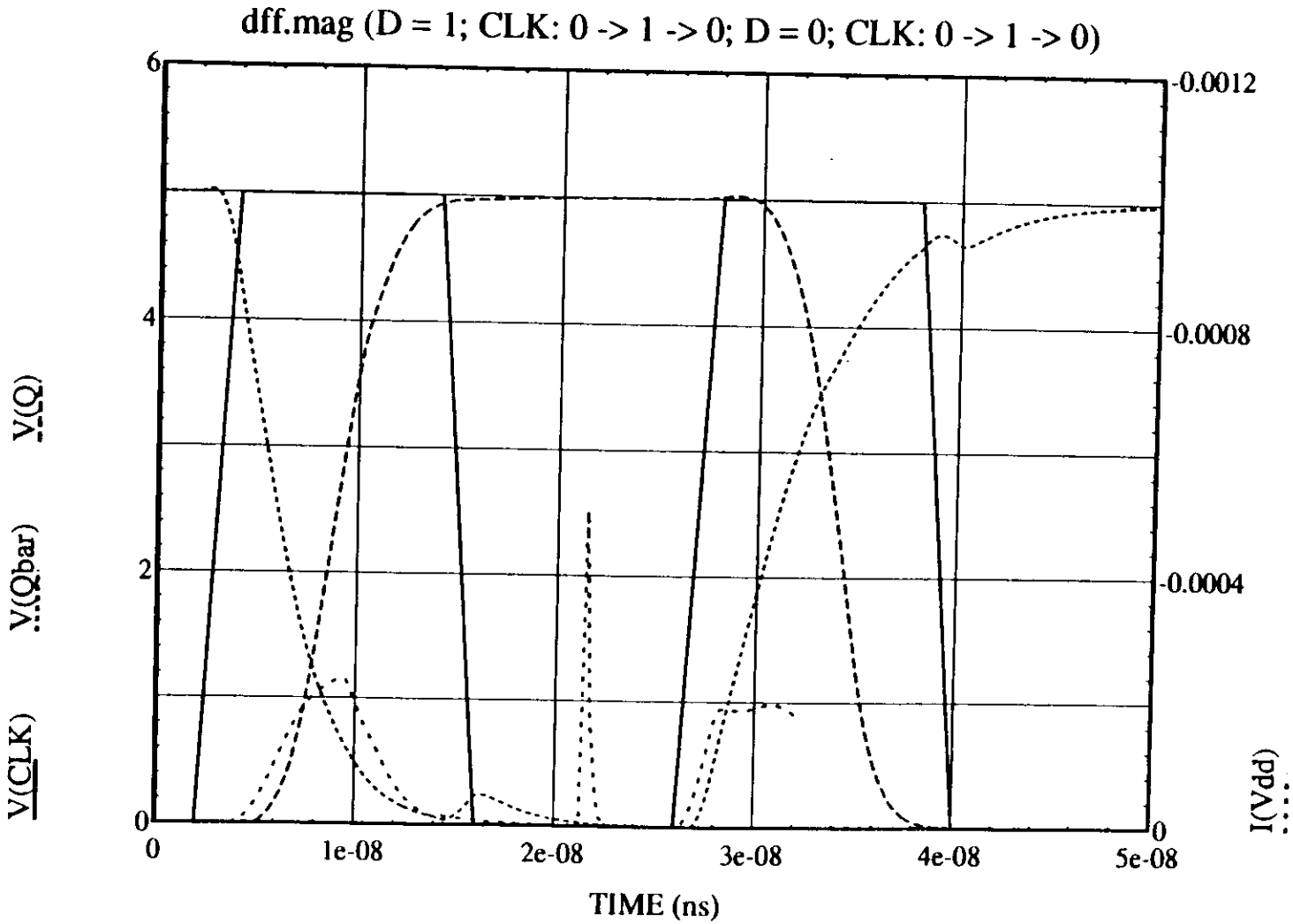

4 bit cpa (AB: 10; C: 1 -> 0 -> 1)
6
4
2
0
0
2e-08
4e-08
6e-08
TIME (ns)
-0.0018
-0.0012
-0.0006
0
V(C)
V(CYbar3)
V(SUMbar3)
I(Vdd)

```
*  Simulation of cell:  inv.fad.mag (A: 0 -> 1 -> 0)                    HERE
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,12ns)
define(TF,2ns)
define(TL,12ns)
define(PER,28ns)
define(TIME,30ns)
*
*
*     /--------------\
*___/       A        \_____________
*
                                                                     HERE
VA  20  0  pulse(0 5 TD TR TF TH PER)
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*
                                                                     HERE
.tran 0.25ns TIME
.print trans v(20) v(21) i(Vdd)
.print trans v(100)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit input (= load)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
                                                                     HERE
XLOAD 2 4 5 21 100 load
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*
                                                                     HERE
include(/ics12/dloh/spice.dir/inv.fad.dir/inv.fad.spice)
*
include(/ics12/dloh/spice.dir/models)
*
.end
```


inv.fad.mag (A: 0 -> 1 -> 0)
6
4
2
0
-0.0012
-0.0008
-0.0004
0
0
1e-08
2e-08
3e-08
TIME (ns)
V(A)
V(B)
I(Vdd)

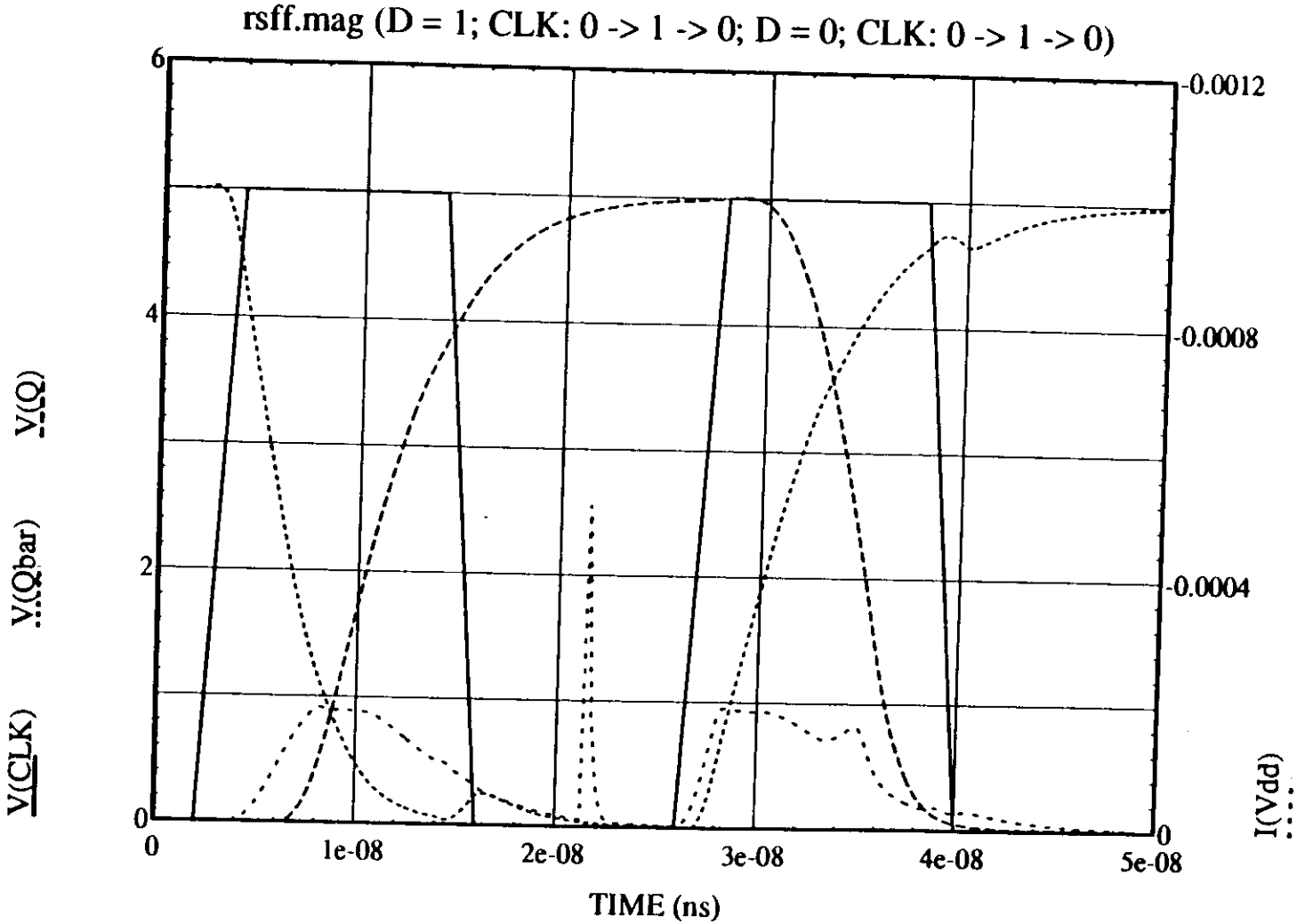
```
*  Simulation of cell:  dff.mag (D = 1; CLK: 0 -> 1 -> 0                    HERE
*                                D = 0; CLK: 0 -> 1 -> 0)
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TDC,2ns)
define(TRC,2ns)
define(THC,10ns)
define(TFC,2ns)
define(TLC,10ns)
define(PERC,24ns)
*
define(TDI,0ns)
define(TRI,0ns)
define(THI,21ns)
define(TFI,0ns)
define(TLI,29ns)
define(PERI,50ns)
*
define(TIME,50ns)
*
*
*      /‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾\                /‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾\
*     /       CLK       \              /       CLK       \
*____/                   \____________/                   \_____________
*
*                  D
*                  |_____________________________________________________
*
VClk      10   0   pulse(0 5 TDC TRC TFC THC PERC)                    HERE
VClkbar   11   0   pulse(5 0 TDC TRC TFC THC PERC)
*
VD        23   0   pulse(0 5 TDI TRI TFI THI PERI)
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*
.nodeset v(43)=5V v(42)=0V                                              HERE
.tran 0.25ns TIME
.print trans v(10) v(43) v(42) i(Vdd)
.print trans v(100) v(101)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit input (= load)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
XLQbar 2 4 5 43 100 load                                                HERE
XLQ    2 4 5 42 101 load
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*
include(/ics12/dloh/spice.dir/dff.dir/dff.spice)                        HERE
*
include(/ics12/dloh/spice.dir/models)
*
```

```
.end
```

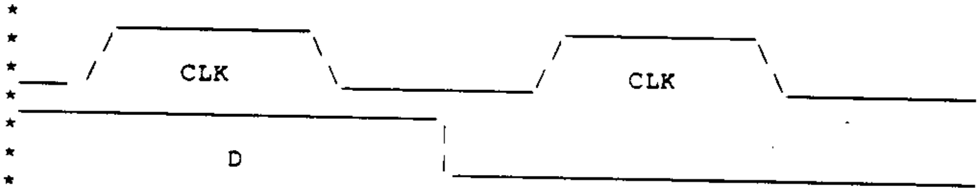

dff.mag (D = 1; CLK: 0 -> 1 -> 0; D = 0; CLK: 0 -> 1 -> 0)
V(CLK)
V(Qbar)
V(Q)
I(Vdd)
6
4
2
0
-0.0012
-0.0008
-0.0004
0
0
1e-08
2e-08
3e-08
4e-08
5e-08
TIME (ns)

```
*  Simulation of cell:  rsff.mag (D = 1; CLK: 0 -> 1 -> 0                HERE
*                                 D = 0; CLK: 0 -> 1 -> 0)
*
*       Notes:  all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TDC,2ns)
define(TRC,2ns)
define(THC,10ns)
define(TFC,2ns)
define(TLC,10ns)
define(PERC,24ns)
*
define(TDI,0ns)
define(TRI,0ns)
define(THI,21ns)
define(TFI,0ns)
define(TLI,29ns)
define(PERI,50ns)
*
define(TIME,50ns)
*
*
*      ____________                ____________
*     /            \              /            \
*____/      CLK     \____________/      CLK     \___________
*
*_____________________|
*                     |
*          D          |_____________________________________
*
VClk      10   0  pulse(0 5 TDC TRC TFC THC PERC)                    HERE
VClkbar   11   0  pulse(5 0 TDC TRC TFC THC PERC)
*
VD        23   0  pulse(0 5 TDI TRI TFI THI PERI)
*
VPRESET   16   0  0V
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*
.nodeset v(43)=5V v(42)=0V                                           HERE
.tran 0.25ns TIME
.print trans v(10) v(43) v(42) i(Vdd)
.print trans v(100) v(101)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit input (= load)
*  Passing Vload Vcmosp Vcmosn output subcktname
*
XLQbar 2 4 5 43 100 load                                             HERE
XLQ    2 4 5 42 101 load
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*                                                                    HERE
include(/ics12/dloh/spice.dir/rsff.dir/rsff.spice)
*
```

```
include(/ics12/dloh/spice.dir/models)
*
.end
```

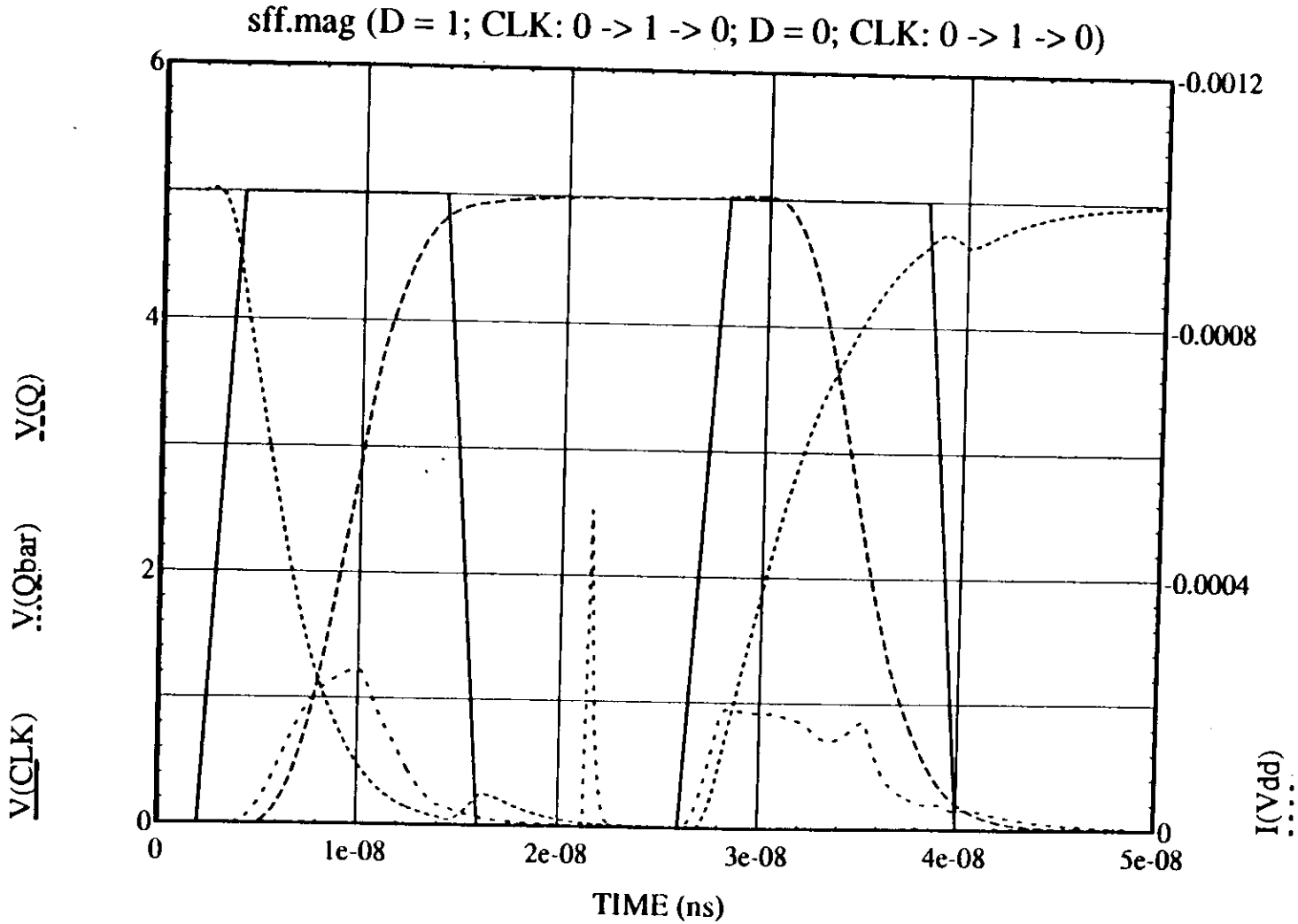

rsff.mag (D = 1; CLK: 0 -> 1 -> 0; D = 0; CLK: 0 -> 1 -> 0)
6
4
2
0
-0.0012
-0.0008
-0.0004
0
0
1e-08
2e-08
3e-08
4e-08
5e-08
TIME (ns)
V(CLK)
V(Qbar)
V(Q)
I(Vdd)

```
 *  Simulation of cell:  sff.mag (D = 1; CLK: 0 -> 1 -> 0          HERE
 *                                D = 0; CLK: 0 -> 1 -> 0)
 *
 *       Notes:  all inputs = 2ns rise/2ns fall
 *               all clocks = 2ns rise/2ns fall
 *               transistors courtesy of sim2spice
 *               all transistor source/drain measurements made by hand
 *               all transistor widths adjusted to Weff of each type
 *                     (Weff = W_drawn - Delta_W)
 *               3 um model cards courtesy of mosis
 *
 *  Cell Inputs
 *
define(TDC,2ns)
define(TRC,2ns)
define(THC,10ns)
define(TFC,2ns)
define(TLC,10ns)
define(PERC,24ns)
*
define(TDI,0ns)
define(TRI,0ns)
define(THI,21ns)
define(TFI,0ns)
define(TLI,29ns)
define(PERI,50ns)
*
define(TIME,50ns)
*
*
```



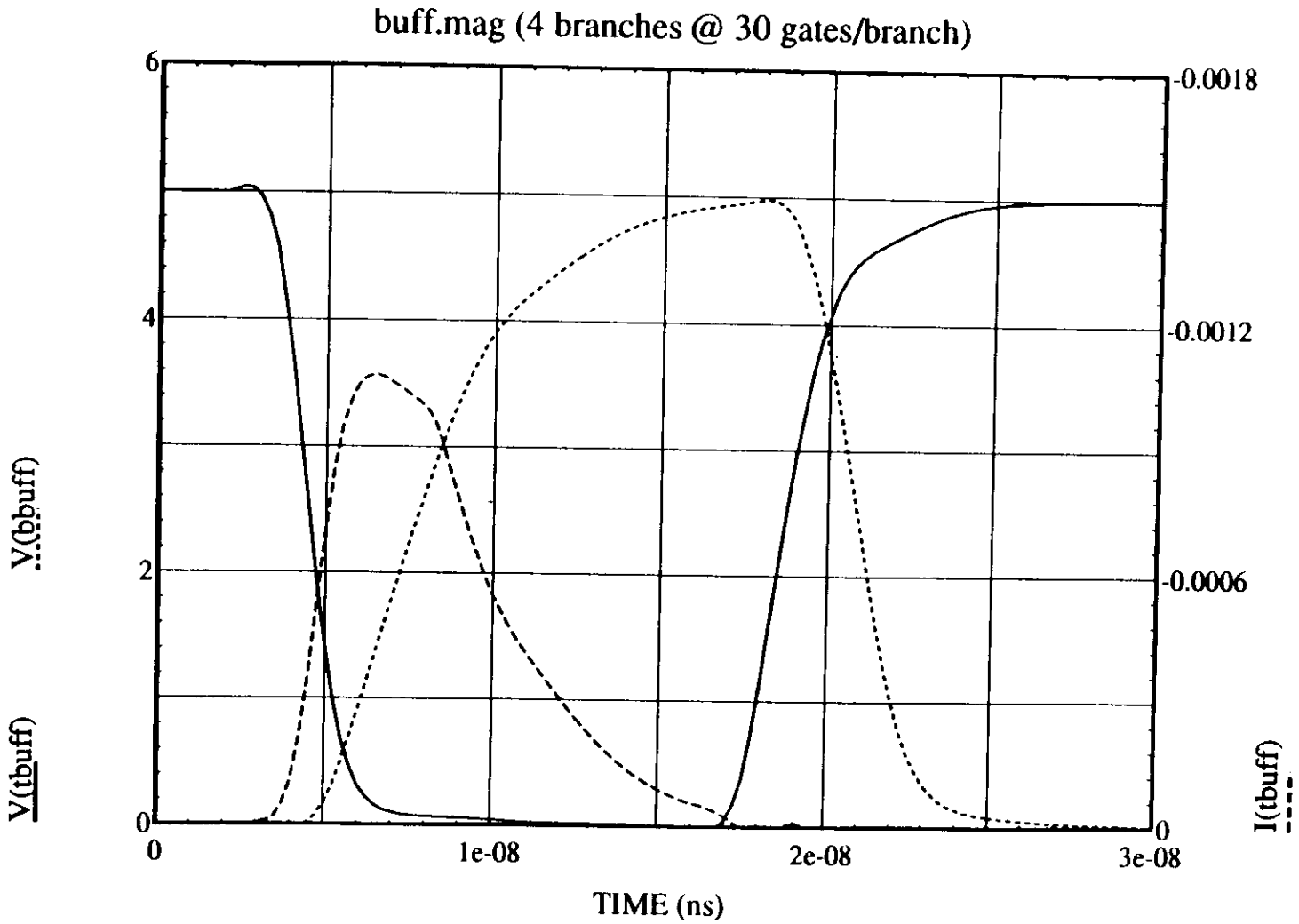

```
*
VClk      10  0  pulse(0 5 TDC TRC TFC THC PERC)          HERE
VClkbar   11  0  pulse(5 0 TDC TRC TFC THC PERC)
*
VD        23  0  pulse(0 5 TDI TRI TFI THI PERI)
*
VPRESET   16  0  0V
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*                                                           HERE
.nodeset v(43)=5V v(42)=0V
.tran 0.25ns TIME
.print trans v(10) v(43) v(42) i(Vdd)
.print trans v(100) v(101)
.options nomod ingold=2
.width out=80
*
*  Pass cell output to subcircuit input (= load)
*  Passing Vload Vcmosp Vcmosn output subcktname
*                                                           HERE
XLQbar 2 4 5 43 100 load
XLQ    2 4 5 42 101 load
*
include(/ics12/dloh/spice.dir/load)
*
include(/ics12/dloh/spice.dir/power)
*                                                           HERE
include(/ics12/dloh/spice.dir/sff.dir/sff.spice)
*
```

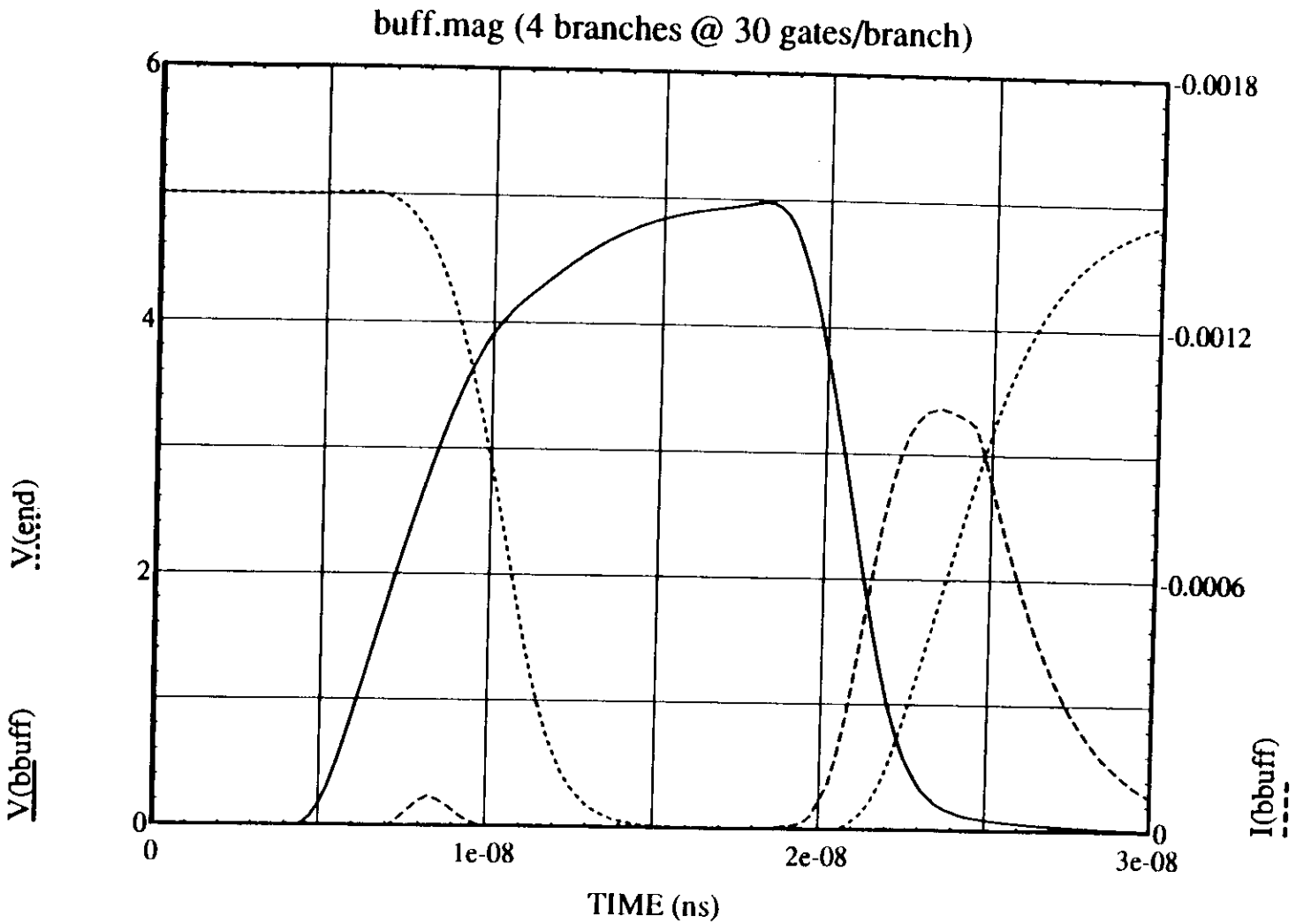
```
include(/ics12/dloh/spice.dir/models)
*
.end
```

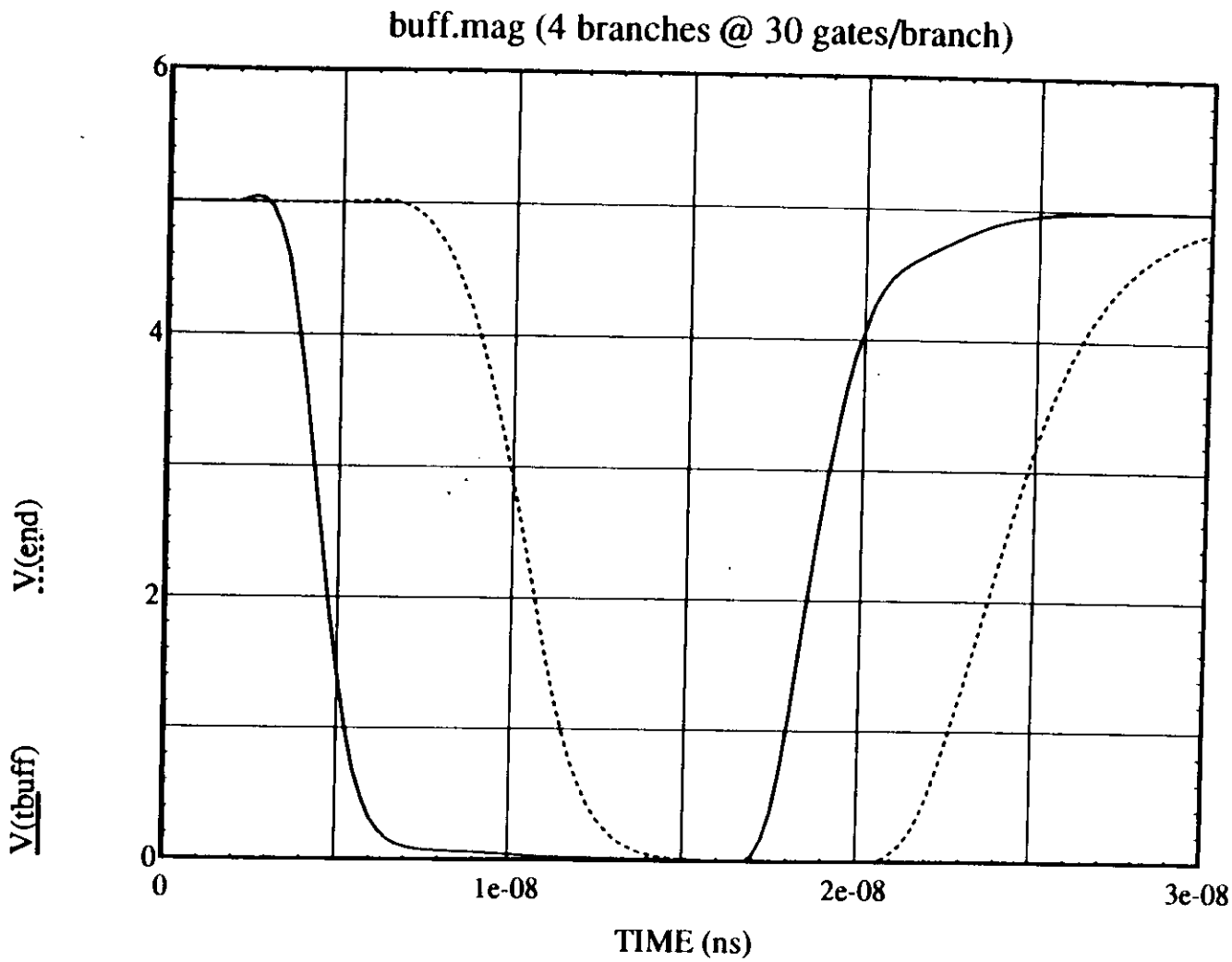

sff.mag (D = 1; CLK: 0 -> 1 -> 0; D = 0; CLK: 0 -> 1 -> 0)
6
4
2
0
-0.0012
-0.0008
-0.0004
0
0
1e-08
2e-08
3e-08
4e-08
5e-08
TIME (ns)
V(CLK)
V(Qbar)
V(Q)
I(Vdd)

```
*  Simulation of cell:  buff.mag (4 branches @ 20 gates)      HERE
*
*       Notes:  buffer transistor widths = 16 lambda
*               simulation of 1 trunk, 4 branches @ 20 gates/branch
*
*               all inputs = 2ns rise/2ns fall
*               all clocks = 2ns rise/2ns fall
*               all transistor source/drain measurements estimated
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,12ns)
define(TF,2ns)
define(TL,12ns)
define(PER,28ns)
define(TIME,30ns)
*
*
*     ____________
*    /            \
*___/       A      \_____________
*
VA  20  0  pulse(0 5 TD TR TF TH PER)                          HERE
*
*  Simulation Outputs
*  Prints inputs, outputs, load output, and current use, respectively
*
*
* v(21) = input to trunk buffer                                 HERE
* v(51) = result at input to branch buffer
* v(53) = result at end of branch
*
.tran 0.25ns TIME
.print trans v(21) v(51) i(Vtbuff)
.print trans v(51) v(53) i(Vbbuff)
.print trans v(21) v(53)
.options nomod ingold=2
.width out=80
*
include(/ics12/dloh/spice.dir/inv.dir/inv.spice)               HERE
*
Xtrunk  2 4 5 21 50 buff
Rtrunk  50 51 60
Ctrunk  51  0 .518pF
*
Xbuffer1  3 4 5 51 52  buff
Xbranch1          52 53  branch20
*
Xbuffer2  1 4 5 51 62  buff
Xbranch2          62 63  branch20
*
Xbuffer3  1 4 5 51 72  buff
Xbranch3          72 73  branch20
*
Xbuffer4  1 4 5 51 82  buff
Xbranch4          82 83  branch20
*
include(/ics12/dloh/spice.dir/buff.dir/buff.spice)
*
include(/ics12/dloh/spice.dir/buff.dir/branch20)
*
include(/ics12/dloh/spice.dir/buff.dir/lump)
```

```
*
*   Standard power, pwell, and substrate voltages
*   Buffer power isolated from standard power by subcircuiting
*
Vdd         1   0   5V
Vtbuff      2   0   5V
Vbbuff      3   0   5V
Vcmosp      4   0   5V
Vcmosn      5   0   0V
*
include(/ics12/dloh/spice.dir/models)
*
.end
```


buff.mag (4 branches @ 30 gates/branch)
6
4
2
0
-0.0018
-0.0012
-0.0006
0
0
1e-08
2e-08
3e-08
TIME (ns)
V(bbuff)
V(tbuff)
I(tbuff)

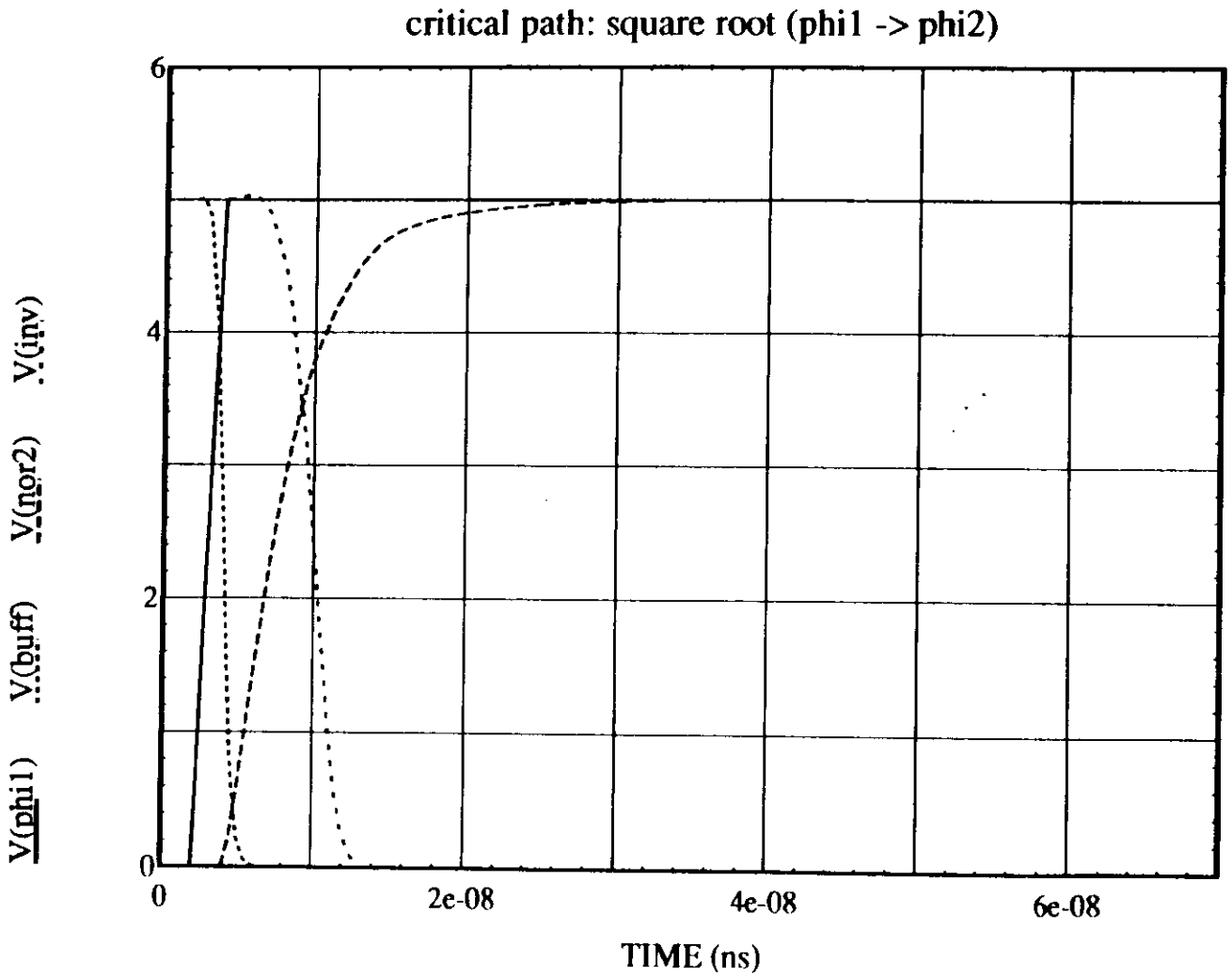

buff.mag (4 branches @ 30 gates/branch)
6
4
2
0
-0.0018
-0.0012
-0.0006
0
0
1e-08
2e-08
3e-08
TIME (ns)
V(end)
V(bbuff)
I(bbuff)

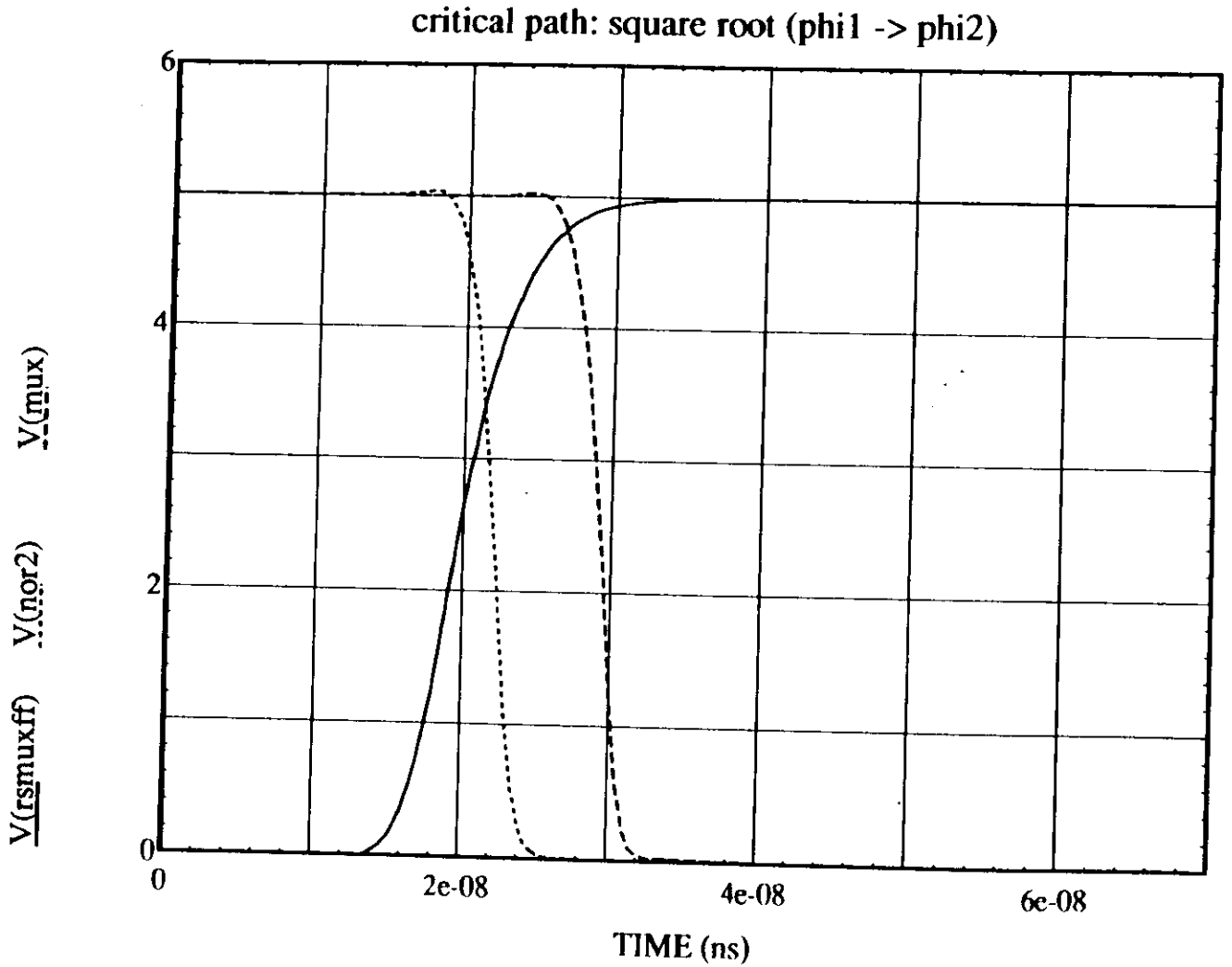

buff.mag (4 branches @ 30 gates/branch)
6
4
2
0
V(end)
V(tbuff)
0
1e-08
2e-08
3e-08
TIME (ns)

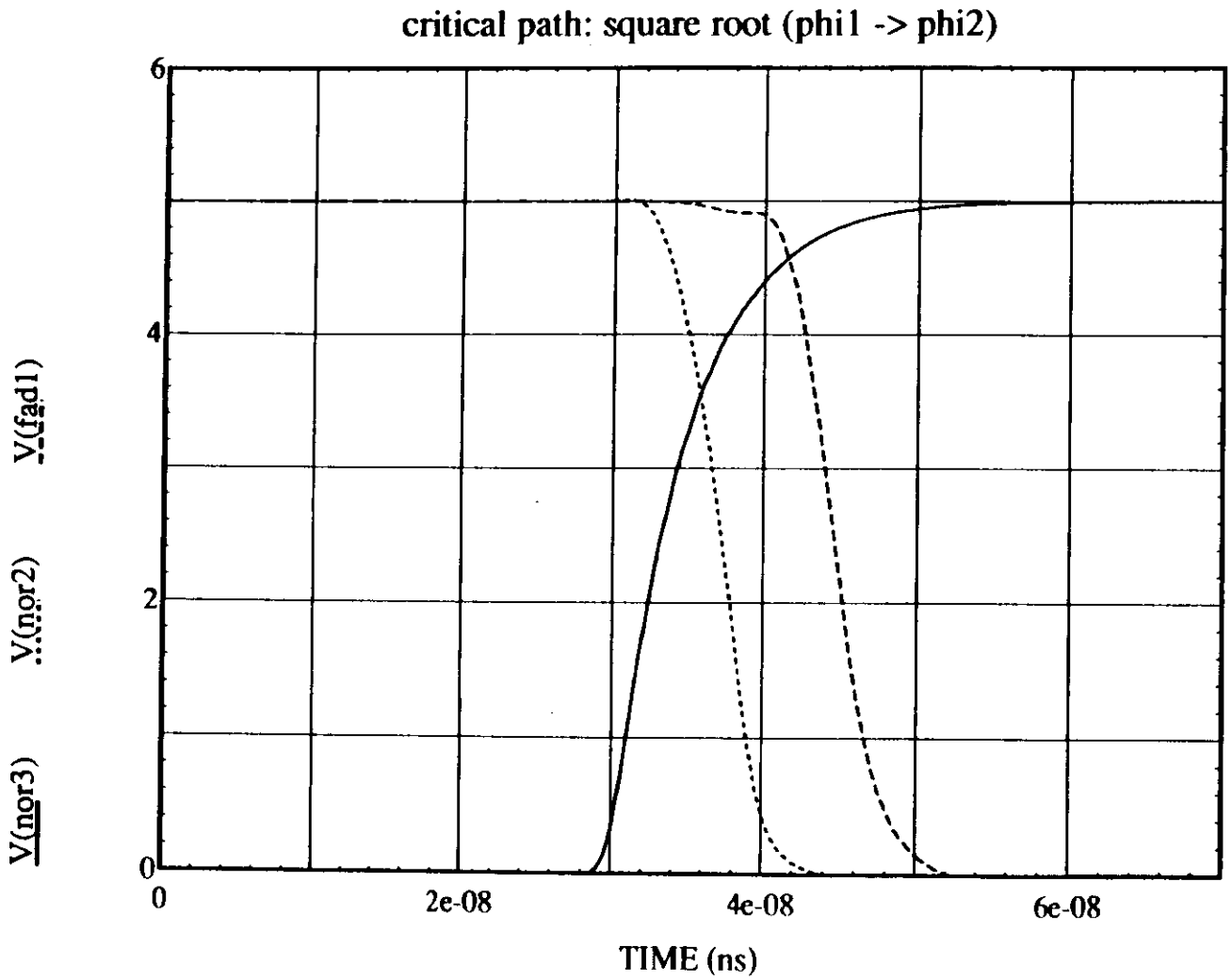
2.2 Spice Results: Final (Critical Paths)

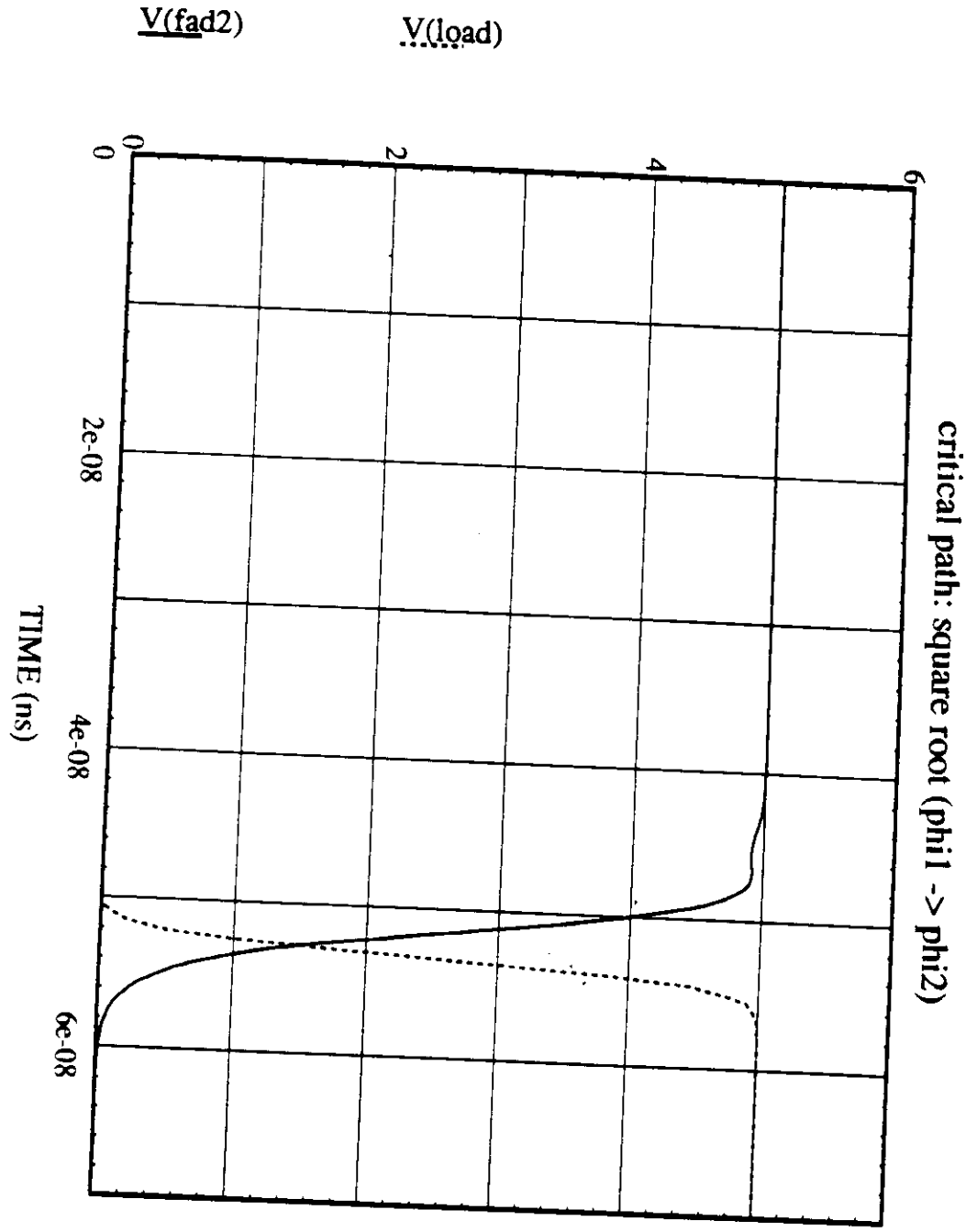
```
*  Simulation of critical path:  critpath (sqr root: phi1 -> phi2)
*
*       Notes:  all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,75ns)
define(TF,2ns)
define(TL,75ns)
define(PER,154ns)
define(TIME,100ns)
*
*
*     ____________
*    /            \
*___/     phi1     \_____________
*
Vphi1      50   0  pulse(0 5 TD TR TF TH PER)
VPRESET    16   0   0
*
*  Simulation Outputs
*
*
.tran 0.5ns TIME                                                HERE
.print trans v(50) v(60) v(61) v(71)
.print trans v(81) v(91) v(101)
.print trans v(111) v(121) v(131)
.print trans v(141) v(151)
.options nomod ingold=2
.nodeset v(51)=5 v(60)=5 v(61)=0 v(71)=5 v(81)=0 v(91)=5
.nodeset v(101)=5 v(111)=0 v(121)=5 v(131)=5 v(141)=5
.width out=80
*
* BUFF          SUBCKT: Vdd Vcmosp Vcmosn A B
* NOR2          SUBCKT: Vdd Vcmosp Vcmosn A B C
* INV           SUBCKT: Vdd Vcmosp Vcmosn A B
* RSMUXFF       SUBCKT: Vdd Vcmosp Vcmosn D0 D1 S Sbar Q Qbar CLK CLKbar PRESET
* MUX           SUBCKT: Vdd Vcmosp Vcmosn D0 D1 S Sbar Q Qbar
* NOR3          SUBCKT: Vdd Vcmosp Vcmosn A B C D
* FAD           SUBCKT: Vdd Vcmosp Vcmosn A B C CYbar SUMbar
*
Xphi1          1 4 5 50 51                          buff
Rbranch        51 60 31
Cbranch        60  0 .24pF
*
Xnor2A         1 4 5 0 60 61                        nor2
Xinv           1 4 5 61 71                          inv
Xrsmuxff       1 4 5 1 0 0 1 81 82 61 71 16         rsmuxff
*
Xnor2B         1 4 5 0 81 91                        nor2
Xmux           1 4 5 91 0 0 1 101 102               mux
Xnor3          1 4 5 0 0 101 111                    nor3
Xnor2c         1 4 5 111 0 121                      nor2
*
Xfad1          1 4 5 0 1 121 132 131                fad
Xfad2          1 4 5 0 1 131 142 141                fad
*
Xload          2 4 5 141 151                        load
*
include(/ics12/dloh/spice.dir/phi1_phi2.dir/subckt.buff)
```

```
include(/icsl2/dloh/spice.dir/phi1_phi2.dir/subckt.nor2)
include(/icsl2/dloh/spice.dir/phi1_phi2.dir/subckt.inv)
include(/icsl2/dloh/spice.dir/phi1_phi2.dir/subckt.rsmuxff)
include(/icsl2/dloh/spice.dir/phi1_phi2.dir/subckt.mux)
include(/icsl2/dloh/spice.dir/phi1_phi2.dir/subckt.nor3)
include(/icsl2/dloh/spice.dir/phi1_phi2.dir/subckt.fad)
*
include(/icsl2/dloh/spice.dir/load)
*
include(/icsl2/dloh/spice.dir/power)
*
include(/icsl2/dloh/spice.dir/models)                    HERE
*
.end
```


critical path: square root (phi1 -> phi2)
6
4
2
0
0
2e-08
4e-08
6e-08
TIME (ns)
V(phi1)
V(buff)
V(nor2)
V(inv)

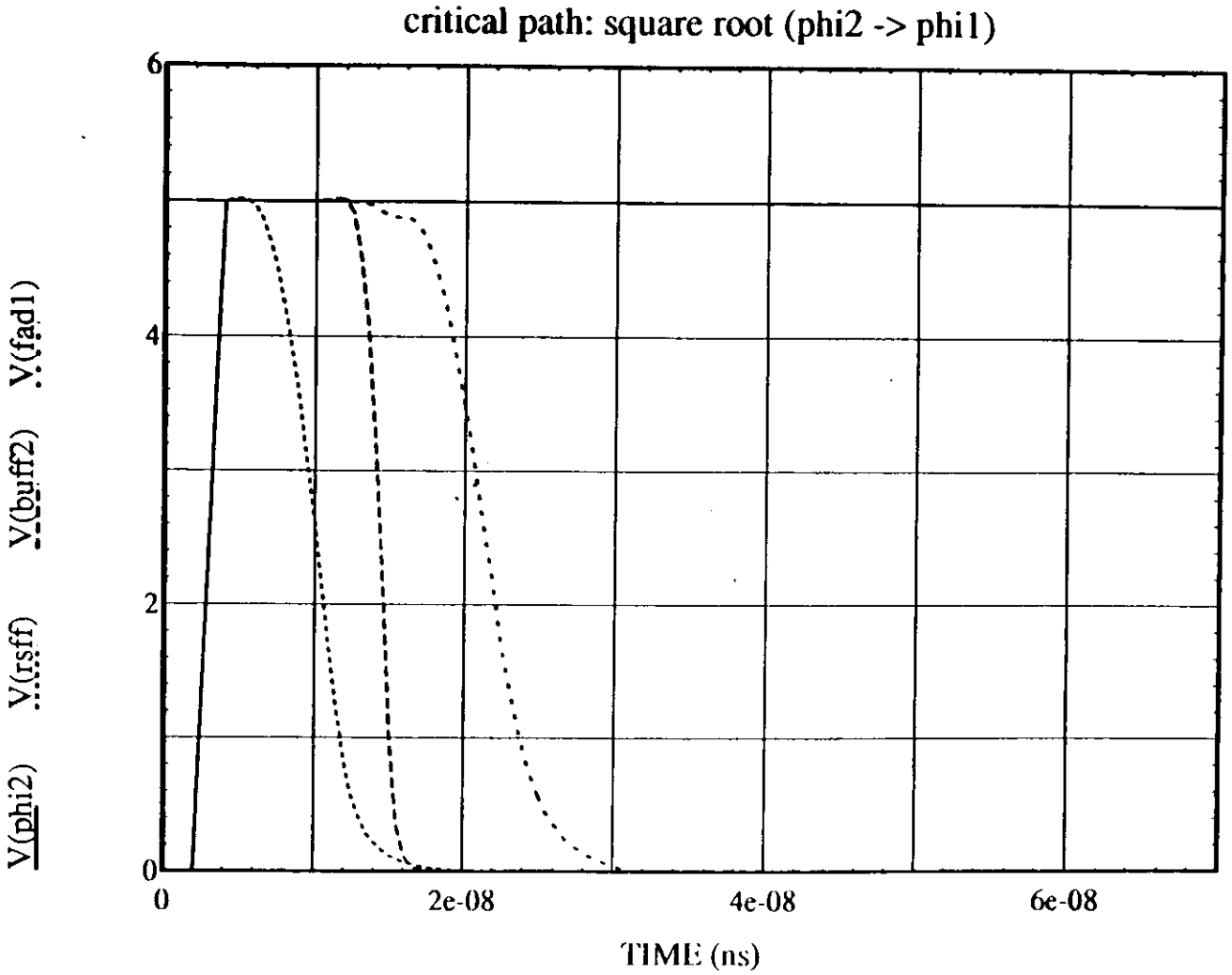

critical path: square root (phi1 -> phi2)
6
4
2
0
0
2e-08
4e-08
6e-08
TIME (ns)
V(rsmuxff)
V(nor2)
V(mux)

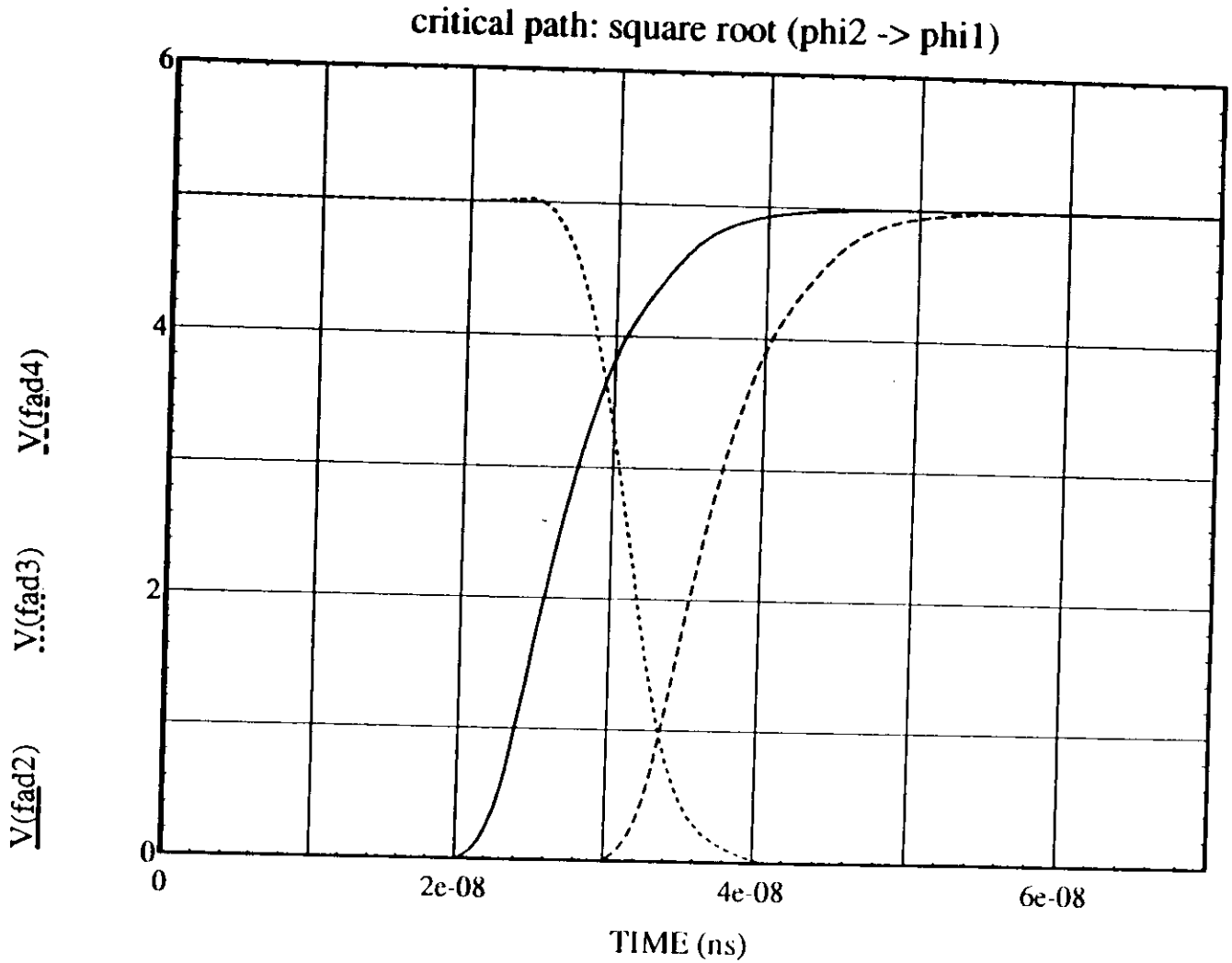

critical path: square root (phi1 -> phi2)
6
4
2
0
0
2e-08
4e-08
6e-08
TIME (ns)
V(fad1)
V(nor2)
V(nor3)

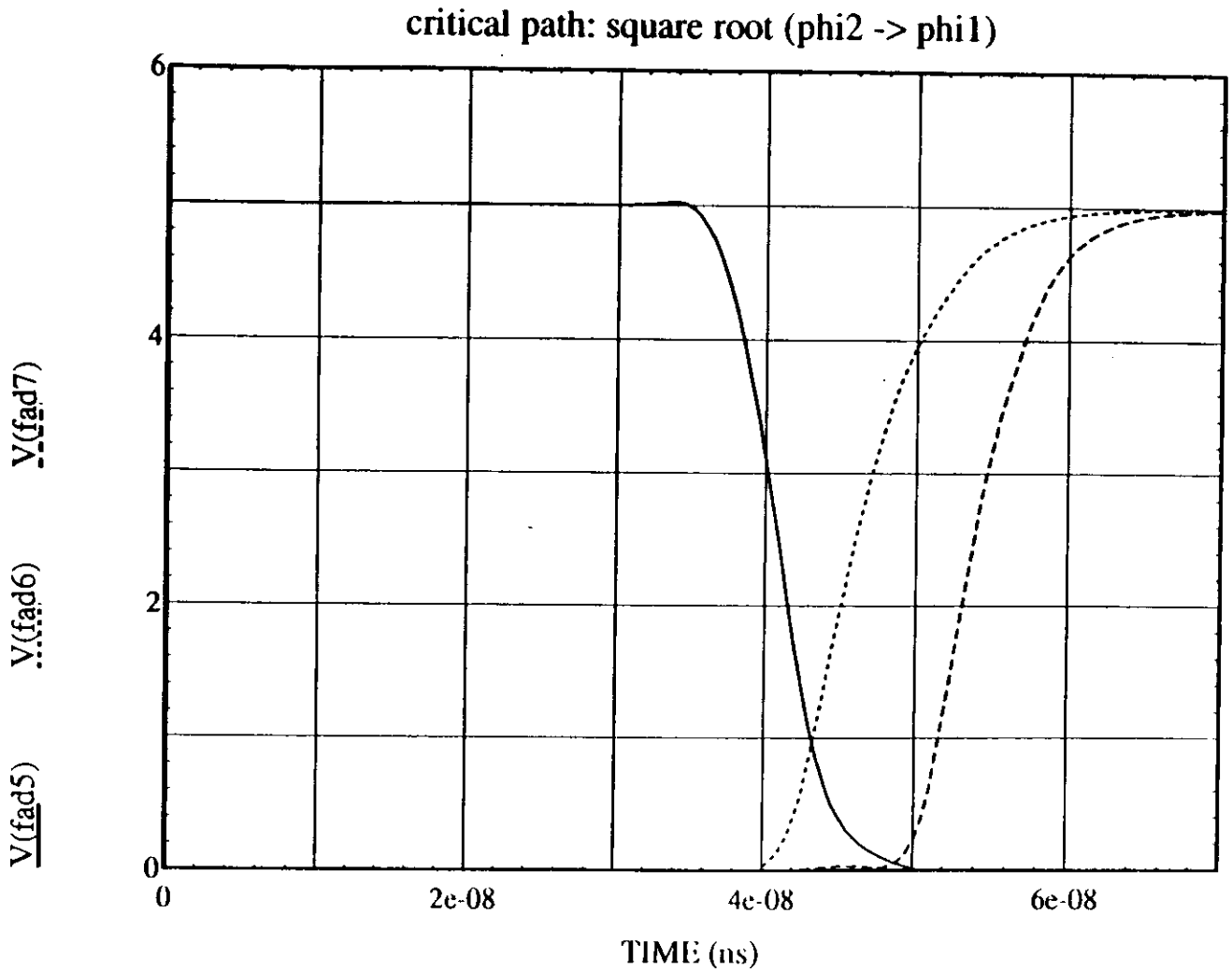

V(fad2)
V(load)
0
2
4
6
0
2e-08
4e-08
6e-08
TIME (ns)
critical path: square root (phi1 -> phi2)

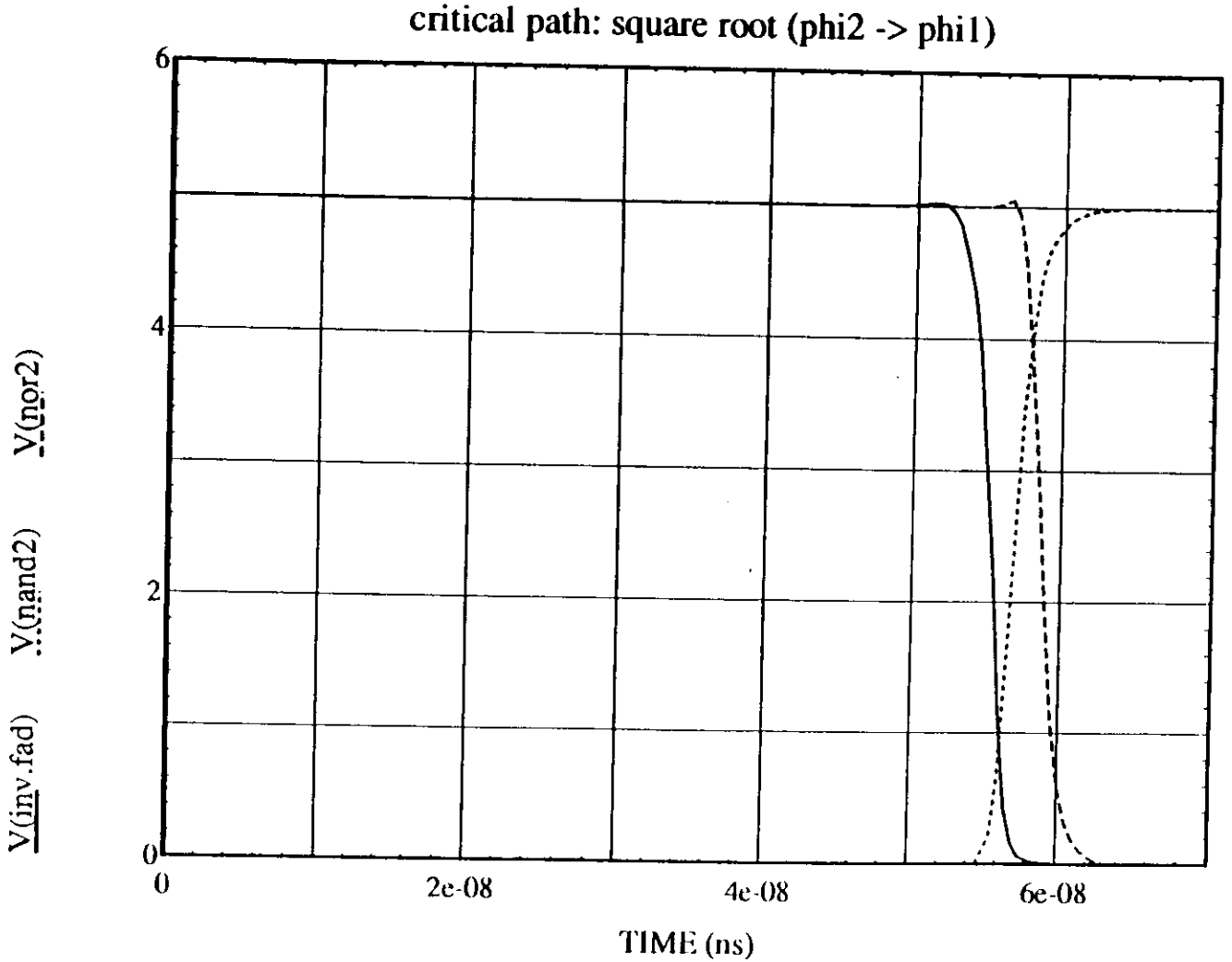
```
*  Simulation of critical path:  critpath (sqr root: phi2 -> phi1)
*
*       Notes:  all clocks = 2ns rise/2ns fall
*               transistors courtesy of sim2spice
*               all transistor source/drain measurements made by hand
*               all transistor widths adjusted to Weff of each type
*                       (Weff = W_drawn - Delta_W)
*               3 um model cards courtesy of mosis
*  Cell Inputs
*
define(TD,2ns)
define(TR,2ns)
define(TH,75ns)
define(TF,2ns)
define(TL,75ns)
define(PER,154ns)
define(TIME,100ns)
*
*
*     ____________
*    /            \
*___/     phi2     \_____________
*
*
*___
*   \    phi2bar     /____________
*    \______________/
*
Vphi2bar  50  0  pulse(5 0 TD TR TF TH PER)                    HERE
Vphi2     60  0  pulse(0 5 TD TR TF TH PER)
VPRESET   16  0  0
*
*  Simulation Outputs
*
*
.tran 0.5ns TIME                                               HERE
.print trans v(60) v(71) v(91) v(102)
.print trans v(111) v(121) v(131)
.print trans v(141) v(151) v(162)
.print trans v(171) v(181) v(191)
.options nomod ingold=2
.nodeset v(71)=5 v(81)=0 v(91)=5 v(102)=5 v(111)=0 v(121)=5 v(131)=0
.nodeset v(141)=5 v(151)=0 v(162)=5 v(171)=0 v(181)=5 v(191)=0
.width out=80
*
* BUFF    SUBCKT: Vdd Vcmosp Vcmosn A B
* RSFF    SUBCKT: Vdd Vcmosp Vcmosn D Q Qbar CLK CLKbar PRESET
* FAD     SUBCKT: Vdd Vcmosp Vcmosn A B C CYbar SUMbar
* INVFAD  SUBCKT: Vdd Vcmosp Vcmosn A B
* NAND2   SUBCKT: Vdd Vcmosp Vcmosn A B C
* NOR2    SUBCKT: Vdd Vcmosp Vcmosn A B C
*
Xphi2bar      1 4 5 50 51                  buff
Xphi2         1 4 5 60 61                  buff
Xrsff         1 4 5  0 71 72 51 61 16      rsff
Xbuff1        1 4 5 71 81                  buff
Rtruck        81 82 25
Ctrunk        82  0 .345pF
Xbuff2        1 4 5 82 91                  buff
Rbranch       91 92 25
Cbranch       92  0 .185pF
*
Xfad1         1 4 5 1 0  92 101 102        fad
Xfad2         1 4 5 1 0 102 111 112        fad
Xfad3         1 4 5 1 0 111 121 122        fad
Xfad4         1 4 5 1 0 121 131 132        fad
Xfad5         1 4 5 1 0 131 141 142        fad
```

```
Xfad6          1 4 5 1 0 141 151 152       fad
Xfad7          1 4 5 1 0 151 161 162       fad
*
Xinvfad        1 4 5 162 171               invfad
Xnand2         1 4 5   1 171 181           nand2
Xnor2          1 4 5   0 181 191           nor2
*
Xload          2 4 5 191 201               load
*
include(/icsl2/dloh/spice.dir/critpath.dir/subckt.buff)
include(/icsl2/dloh/spice.dir/critpath.dir/subckt.rsff)
include(/icsl2/dloh/spice.dir/critpath.dir/subckt.fad)
include(/icsl2/dloh/spice.dir/critpath.dir/subckt.inv.fad)
include(/icsl2/dloh/spice.dir/critpath.dir/subckt.nand2)
include(/icsl2/dloh/spice.dir/critpath.dir/subckt.nor2)
*
include(/icsl2/dloh/spice.dir/load)
*
include(/icsl2/dloh/spice.dir/power)
*                                                          HERE
include(/icsl2/dloh/spice.dir/models)
*
.end
```


critical path: square root (phi2 -> phi1)
V(phi2)
V(rsff)
V(buff2)
V(fad1)
6
4
2
0
0
2e-08
4e-08
6e-08
TIME (ns)


critical path: square root (phi2 -> phi1)
6
4
2
0
0
2e-08
4e-08
6e-08
TIME (ns)
V(fad2)
V(fad3)
V(fad4)


critical path: square root (phi2 -> phi1)
6
4
2
0
0
2e-08
4e-08
6e-08
TIME (ns)
V(fad5)
V(fad6)
V(fad7)


critical path: square root (phi2 -> phi1)
V(inv.fad)
V(nand2)
V(nor2)
6
4
2
0
0
2e-08
4e-08
6e-08
TIME (ns)