WAVEFORM BOUNDS FOR LINEAR RC MESH CIRCUITS WITH LEAKAGE PATHS TO THE GROUND

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Abstract - We demonstrate that a certain class of *RC* circuits with leakage paths to the ground do exhibit monotonic behavior under one condition. We can therefore apply a variant of Penfield's [3] waveform bounding inequality to this class of circuits. An example is provided to illustrate the method.

I. Background and Notation

In [5], Zukowski mentioned that Penfield's [3] waveform bounding double inequality is applicable only for zero state step response of *RC* circuits. We suggest that a variant of Penfield's bounding inequality can be used to treat a type *RC* circuits with leakage paths to the ground. The general nodal equation for this class of *RC* circuits is

$$\mathbf{C}\ \dot{\mathrm{v}}(t) = \mathbf{G}\ \mathrm{v}(t) + \mathbf{d}\ e(t), \tag{1}$$

where $\mathbf{C}$ is the capacitance (diagonal) matrix, $\mathrm{v}(t)$ is a vector of node voltage at each capacitor, $\dot{\mathrm{v}}(t)$ is the time derivative of $\mathrm{v}(t)$, $\mathbf{d}$ is the conductance with d_i representing the conductance connected from node n_i to the excitation source $e(t)$. $\mathbf{G}$ is the node-conductance matrix with components G_{ij}. For $j \neq i$, G_{ij} is the branch conductance between nodes n_i and n_j, whereas G_{ii} is the negative sum of all branch conductances at node n_i. For $j \neq i$, G_{ij} is equal to G_{ji} by reciprocity, therefore $-\mathbf{G}$ is a *Stieltjes matrix* [1]. Since $-\mathbf{G}$ is an *essentially nonnegative matrix*, $-\mathbf{G}$ is inverse-positive. This allows us to define $\mathbf{R} \equiv -\mathbf{G}^{-1}$. If $e(t)$ is a unit step function, we can write (1) as

$$\mathbf{RC}\ \dot{\mathrm{v}}(t) = \mathrm{v}(\infty) - \mathrm{v}(t), \tag{2}$$

where $\mathrm{v}(0)$ and $\mathrm{v}(\infty)$ represent the initial and final voltages across capacitors, respectively. The final voltage $\mathrm{v}(\infty) = \mathbf{Rd}$ is equal to $\mathbf{1}$ for *RC* circuits without leakage path to the ground; otherwise $\mathrm{v}(\infty) = \mathbf{Rd} < \mathbf{1}$. Since $-\mathbf{G}$ is inverse-positive, as pointed out in [4], $R_{ii}R_{jk} - R_{ki}R_{ji} \geq 0$.

Moreover, we realize that $e^{\mathbf{C}^{-1}\mathbf{G}t} \geq 0$ [2], which implies that the impulse response of the circuit is nonnegative. Therefore, if $v_j(0) \geq v_j(\infty)$, we expect each node voltage $v_j(t)$ to be a nonincreasing function of time. In other words, $\frac{dv_j}{dt} \leq 0$, and it follows that

$$\sum_j (R_{ii}R_{jk} - R_{ki}R_{ji})C_j \frac{dv_j}{dt} \leq 0 \,. \tag{3}$$

II. Main Result

From (3), we now derive a double inequality for $v_i(t)$. Most of the derivations are identical to that presented in [3] and will not be repeated here. Only parts which differ will be pointed out. From (3), the concavity inequality for the class of RC circuits that we are considering is

$$R_{ii}[v_k(\infty) - v_k(t)] \leq R_{ki}[v_i(\infty) - v_i(t)] \,. \tag{4}$$

Moreover, we define $f_i(t)$ as

$$f_i(t) = T_{Di} + \sum_k R_{ki}C_k[v_k(0) - v_k(\infty)] + \int_0^t (v_i(\infty) - v_i(t'))dt' \,. \tag{5}$$

This definition of $f_i(t)$ coincides with what is defined in (10) of [3] when $v_k(\infty) = 1$ and $v_k(0) = 0$; which is the limiting case that they have considered. The rest of the derivations are identical to [3]. We derive the upper inequality to be

$$\frac{\sum_k R_{ki}C_k[v_k(0) - v_k(\infty)]}{T_P} e^{\frac{T_P - T_{Ri}}{T_P}} e^{-\frac{t}{T_P}} + v_i(\infty) \geq v_i(t) \,, \tag{6.a}$$

which holds for $t \geq T_P - T_{Ri}$. The lower inequality is

$$v_i(t) \geq \frac{\sum_k R_{ki}C_k[v_k(0) - v_k(\infty)] + (T_{Di} - T_{Ri})[v_i(\infty) - v_i(0)]}{T_P} e^{\frac{T_{Di} - T_{Ri}}{T_{Ri}}} e^{-\frac{t}{T_{Ri}}} + v_i(\infty) \,, \tag{6.b}$$

and it holds for $t \geq T_{Di} - T_{Ri}$. This double inequality is valid for arbitrary initial and final conditions and coincides with Penfield's bounding inequality when $v_k(0) = 0$ and $v_k(\infty) = 1$.

III. An Example

Consider the following nMOS implementation of an *AND* gate,

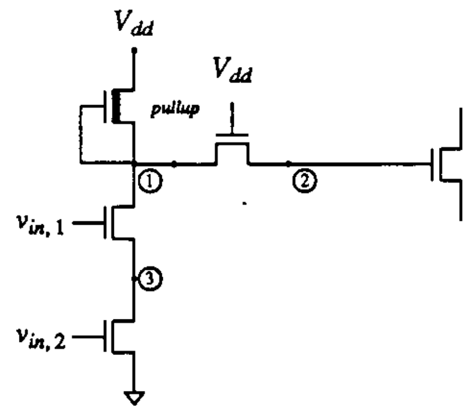

Fig. 1.a. An nMOS AND Gate.

with $v_{in,1} = v_{in,2} = 1$. The *RC* circuit model of this *AND* gate is given by

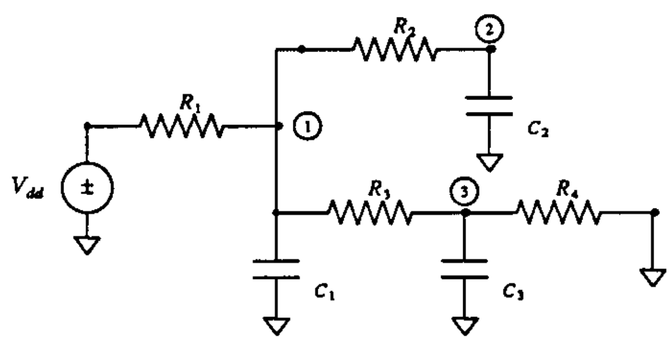

Fig. 1.b. The *RC* Equivalent Circuit.

If $V_{dd} = 1$, equation (1) becomes

$$\begin{bmatrix} C_1 & 0 & 0 \\ 0 & C_2 & 0 \\ 0 & 0 & C_3 \end{bmatrix} \begin{bmatrix} \dot{v}_1(t) \\ \dot{v}_2(t) \\ \dot{v}_3(t) \end{bmatrix} = \begin{bmatrix} -(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}) & \frac{1}{R_2} & \frac{1}{R_3} \\ \frac{1}{R_2} & -\frac{1}{R_2} & 0 \\ \frac{1}{R_3} & 0 & -(\frac{1}{R_3}+\frac{1}{R_4}) \end{bmatrix} \begin{bmatrix} v_1(t) \\ v_2(t) \\ v_3(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{R_1} \\ 0 \\ 0 \end{bmatrix} u(t) ,$$

or

$$\mathbf{RC}\,\dot{\mathbf{v}}(t) = \mathbf{v}(\infty) - \mathbf{v}(t),$$

where

$$\mathbf{R} = \begin{bmatrix} \frac{R_1(R_3+R_4)}{R_1+R_3+R_4} & \frac{R_1(R_3+R_4)}{R_1+R_3+R_4} & \frac{R_1R_4}{R_1+R_3+R_4} \\ \frac{R_1(R_3+R_4)}{R_1+R_3+R_4} & R_2+\frac{R_1(R_3+R_4)}{R_1+R_3+R_4} & \frac{R_1R_4}{R_1+R_3+R_4} \\ \frac{R_1R_4}{R_1+R_3+R_4} & \frac{R_1R_4}{R_1+R_3+R_4} & \frac{R_4(R_1+R_3)}{R_1+R_3+R_4} \end{bmatrix},$$

and

$$\mathbf{v}(\infty) = \begin{bmatrix} \frac{R_3+R_4}{R_1+R_3+R_4} \\ \frac{R_3+R_4}{R_1+R_3+R_4} \\ \frac{R_4}{R_1+R_3+R_4} \end{bmatrix}.$$

We substitute numerical values $R_1 = 40\,K\Omega$, $R_2 = 2.5\,K\Omega$, $R_3 = 5\,K\Omega$, $R_4 = 5\,K\Omega$, $C_1 = 1.6\times10^{-2}\,pF$, $C_2 = 0.6\times10^{-2}\,pF$, and $C_3 = 1.6\times10^{-2}\,pF$ into (6). The solid line in Fig. 2 is the exact solution of the RC circuit, depicting the behavior of $v_1(t)$ discharging from initial conditions $v_k(0) = 1$; k=1,2,3. The dotted lines are the responses suggested by the bounding inequality.

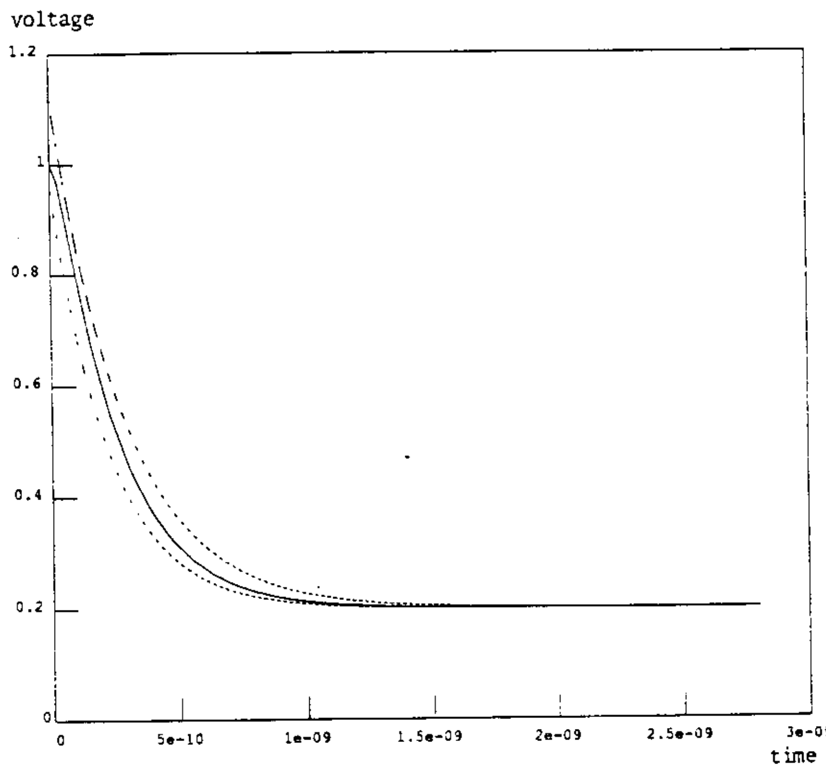

Fig. 2. The Response of $v_1(t)$.

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