AN EXTENSION OF ELMORE'S DELAY

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Abstract - This work extends the notion of delay defined by Elmore [2] to accommodate the effect of non-unit-step (slow) excitations. A single value of delay for any node in an *RC* network is derived by using a state-space model. This model provides a compact delay expression in closed-form. It also handles multiple sources of excitation, and we show that delay estimation for slow excitations is no harder than for unit-step input.

I. Introduction

According to Pederson [7], "timing simulation is circuit simulation in which approximations are purposely introduced with relaxed accuracy to achieve greatly improved simulation speed." We are trying to tackle a problem in the area of logic-level timing simulation of digital MOS/LSI circuits: finding the *delay* at any node of a digital MOS circuit modeled by an *RC* network. Chronologically, Penfield et al. in 1981 derived formulas to bound the waveforms of node voltages in an *RC* network [6]. Five restrictions were imposed in their approach: 1) conducting transistors are modeled as linear resistors, 2) only one source is driving the *RC* network, 3) input to the *RC* network is a unit-step function, 4) only *RC* tree networks are considered, and 5) initial charges on capacitors are only considered as a special case in which an *RC* tree without any initial charge is driven through another *RC* tree that is initially fully charged. Based on these restrictions, Penfield et al. suggested a very efficient $O(N)$ algorithm to bound the waveform for any node voltage in an *RC* tree network with N capacitors. In 1984, Lin et al. considered delay in *RC* mesh networks with arbitrary initial charge distribution. The first three restrictions assumed by Penfield et al. were also made in Lin's approach [4]. He proposed a relaxation algorithm for expressing delays in an *RC* mesh network in terms of a set of simultaneous linear equations. In 1985, Wyatt [12] showed that Penfield's wave bounding formulas are also applicable to *RC* mesh networks.

Here we attempt to relax the last four restrictions by finding delays based on a state-space model of the *RC* network. We follow the linear switch-level model of MOS transistors proposed by Bryant, Terman and others [1, 10, 6, 4, 5, 12]. In this model, a transistor is parameterized in terms of *resistance R* and a capacitor by *capacitance C*. Input resistance of an MOS transistor is assumed to be infinite. Therefore, the delay analysis of an MOS circuit can be reduced to that of *RC* networks. Furthermore, since we are analyzing digital MOS circuits, the class of *RC* networks are those where there is a capacitor between every node and ground. The analysis of MOS/LSI digital circuits is therefore equivalent to the analysis of *stages* [5] of disjoint *RC* networks.

II. An Extension of Elmore's Delay

Delay is the manifestation of the inertia of a system. One way to quantify delay as suggested by Elmore [2] is to take the first-order moment of the impulse response $h(t)$, commonly known as the inertia, as the delay, i.e.,

$$T_D \equiv \int_0^\infty h(t)t \; dt. \tag{1}$$

To extend the above definition of delay for each node n_i of an *RC* network we attach a subscript i to T_D and $h(t)$ of the above definition and obtain,

$$T_{Di} \equiv \int_0^\infty h_i(t)t \; dt = \int_0^\infty (u(t) - v_i(t)) \, dt \; ,$$

where $h_i(t)$ is the impulse response at node n_i, and $v_i(t)$ is the voltage at n_i due to the unit-step excitation $u(t)$. However, the quantity defined in (1) is solely a measure of the inertia of a system, and therefore is not a good definition of *delay* in the electrical sense. For instance, it does not account for extrinsic factors such as different input waveforms which may result different delays. Nor does it care for intrinsic factors like initial conditions. Therefore, Elmore's definition of delay is inadequate for those stages of *RC* networks where the output produced by one stage is the input to another *RC* network at the next stage. We extend Elmore's definition of delay to cover both extrinsic and intrinsic factors. Namely, delay is defined to be the difference in areas covered by $u(t)$ and $x_i(t)$ along time, i.e.,

$$T_{Di} \equiv \int_0^\infty (u(t) - x_i(t)) \, dt. \tag{2}$$

where $x_i(t)$ is the voltage at n_i due to excitation $e(t)$ which is not necessarily an unit-step function. Clearly, (2) converges to (1) when $e(t)$ is a unit-step function. A convenient way to express

delay for all nodes in the network is to use the vector notation:

$$\mathbf{T}_D \equiv \int_0^\infty (\mathbf{u}(t) - \mathbf{x}(t))\, dt. \tag{3}$$

By taking the Laplace transform on both sides of (3) and taking their limits as s approaches zero, we obtain,

$$\mathbf{T}_D = \lim_{s \to 0} (\mathbf{u}(s) - \mathbf{x}(s)). \tag{4}$$

It will be shown in the following section that (4) is indeed a consistent definition of delay.

III. A State-Space Model for RC Networks

The state-space approach involves considering the voltage $x_i(t)$ at each capacitor (w.r.t. ground) as state variable. The state equation is presented as a system of linear differential equations:

$$\mathbf{C}\, \dot{\mathbf{x}}(t) = \mathbf{G}\, \mathbf{x}(t) + \mathbf{D}\, \mathbf{e}(t), \tag{5}$$

where $\mathbf{C}$ is the capacitance (diagonal) matrix, $\mathbf{x}(t)$ is the state vector, $\dot{\mathbf{x}}(t)$ is the time derivative of $\mathbf{x}(t)$, $\mathbf{D}$ is the conductance (diagonal) matrix with D_{ii} representing the conductance connected from node n_i to excitation source $e_i(t)$; D_{kk} and $e_k(t)$ are zero if there is no excitation source connected to node n_k. $\mathbf{G}$ is the node-conductance matrix with components G_{ij}. For $j \neq i$, G_{ij} is the branch conductance between nodes n_i and n_j, whereas G_{ii} is the negative sum of all branch conductances at node n_i. For $j \neq i$, G_{ij} is equal to G_{ji} by symmetry, therefore $-\mathbf{G}$ is a *Stieltjes matrix*. This formulation is sufficiently general to include both tree and mesh *RC* networks.

To measure the delay of a node in an *RC* network, it suffices to consider the normalized case where the node voltage starts from some initial value $x_i(0)$ between 0 and 1, and is driven towards the final value 1. The results obtained in this normalized case are easily adapted to both charging and discharging processes (final value 0), and to any values of supply voltage. Rewriting (5) as,

$$\dot{\mathbf{x}}(t) = \mathbf{A}\, \mathbf{x}(t) + \mathbf{B}\, \mathbf{e}(t), \tag{6}$$

where $\mathbf{A} \equiv \mathbf{C}^{-1}\, \mathbf{G}$ and $\mathbf{B} \equiv \mathbf{C}^{-1}\, \mathbf{D}$. Applying the Laplace transform on both sides of (6), and substituting the Laplace transform of $\mathbf{x}(t)$ into (3) gives us:

$$\mathbf{T}_d = \lim_{s \to 0} \left(\mathbf{u}(s) - (s\mathbf{I} - \mathbf{A})^{-1} \left(\mathbf{B}\mathbf{e}(s) + \mathbf{x}(0)\right)\right),$$

where $\mathbf{e}(s)$ is the Laplace transform of $\mathbf{e}(t)$ and $\mathbf{x}(0)$ are the initial voltages on the capacitors. The inverse of the characteristic function of $\mathbf{A}$ can be expanded at the origin as an infinite geometric series, giving us,

$$\mathbf{T}_d = \lim_{s \to 0} \left(\mathbf{u}(s) + (\mathbf{A}^{-1} + s\mathbf{A}^{-2} + s^2\mathbf{A}^{-3} + \cdots)\left(\mathbf{B}\mathbf{e}(s) + \mathbf{x}(0)\right)\right). \tag{7}$$

The existence of $\mathbf{A}^{-1}$ (which is equal to $\mathbf{G}^{-1}\mathbf{C}$) is guaranteed by the fact that $-\mathbf{G}$ is a *Stieltjes matrix*. For input functions that stay sufficiently long, all capacitors in the *RC* network will be eventually charged to unit voltage. This means that $\mathbf{A}\mathbf{1} + \mathbf{B}\mathbf{e}(\infty) = \mathbf{0}$, or $\lim_{s \to 0} s\mathbf{A}^{-1}\mathbf{B}\mathbf{e}(s) = -\mathbf{1}$. The condition $\mathbf{A}^{-1}\mathbf{B}\mathbf{1} = -\mathbf{1}$ is another way to say that the *RC* network has no d.c. path to ground. Therefore, (7) can be reduced to:

$$\mathbf{T}_d = \mathbf{A}^{-1}\left[\mathbf{x}(0) - \mathbf{1}\right] + \lim_{s \to 0}\left[\mathbf{u}(s) + \mathbf{A}^{-1}\mathbf{B}\mathbf{e}(s)\right]. \tag{8}$$

The first term is the *intrinsic delay* because it accounts for the delay due to the intrinsic characteristics (circuit topology and initial conditions) of an *RC* network. The second term is the *extrinsic delay* since it measures the differences between external excitations and the unit-step function. Expression (8) reduces to Elmore's definition of delay when all input excitations are unit-steps.

Expression (8) is sufficiently general to handle arbitrary input and arbitrary distribution of initial charges. The problem of estimating delays for all nodes is therefore shown to boil down to finding the inverse of the node-conductance matrix $\mathbf{G}$, and evaluating $\lim_{s \to 0}\left[\mathbf{u}(s) + \mathbf{A}^{-1}\mathbf{B}\mathbf{e}(s)\right]$. By rewriting (5) as

$$\mathbf{G}^{-1}\mathbf{C}\,\dot{\mathbf{x}}(t) = \mathbf{x}(t) + \mathbf{G}^{-1}\mathbf{D}\mathbf{e}(t),$$

or

$$\mathbf{R}\mathbf{C}\,\dot{\mathbf{x}}(t) = -\mathbf{A}^{-1}\mathbf{B}\mathbf{e}(t) - \mathbf{x}(t), \tag{9}$$

we notice that equation (9) is the mesh equation for an *RC* network, $\mathbf{R} \equiv -\mathbf{G}^{-1}$ is therefore the resistance matrix. By reciprocity, R_{ii} is the driving point resistance observed at node n_i with all the voltage sources grounded and all capacitors removed. For $i \neq j$, R_{ij} is therefore the transresistance which is common between n_i and n_j. As $-\mathbf{G}$, $\mathbf{R}$ is also symmetric and positive definite. Here are two ways of finding $\mathbf{R} = -\mathbf{G}^{-1}$. First, in [8] topological formulas for finding the driving point resistance R_{ij} are suggested. Second, we can factorize $\mathbf{G}$ into product of two triangular matrices where one is the transpose of the other (Cholesky decomposition) [9]. The inverse of $\mathbf{G}$

can then be found readily by finding the inverse of any one of the triangular matrices. This numerical method takes $O(N^3)$ floating-point operations. In terms of computational complexity, this apparently agrees with Lin's [4] result in which his delay estimation algorithm has to solve a system of linear equations.

Without loss of generality, we now focus on *RC* networks with only one type of excitation $e(t)$, for the sake of simplicity for presentation. The state equation for this case is: $\dot{\mathbf{x}}(t) = \mathbf{A}\,\mathbf{x}(t) + \mathbf{b}\,e(t)$, where $\mathbf{A}^{-1}\mathbf{b} = -\mathbf{1}$. Hence, we can rewrite equation (8) as,

$$\mathbf{T}_d = \mathbf{RC}\,[\,\mathbf{1} - \mathbf{x}(0)\,] + \lim_{s \to 0}\,[\,\mathbf{u}(s) - \mathbf{1}e(s)\,]. \tag{10}$$

IV. Stages of RC Networks

We assume that a digital MOS/LSI circuit can be decomposed into *stages* [5] of *RC* networks, where the output produced by one stage is the input to the next stage. We denote $\mathbf{T}_d^{[i]}$ as the delay expression at stage i, $\mathbf{R}^{[i]}\mathbf{C}^{[i]}$ as the *RC* matrices at stage i, and $H^{[i]}(s)$ as the transfer function of a node at stage i where its signal is fed as input to stage $i+1$. Elmore's delay at this particular node is denoted by $T_c^{[i]}$. Without loss of generality, we assume that the excitation at the first stage is a unit-step, i.e., $e^{[1]}(s) = \frac{1}{s}$.

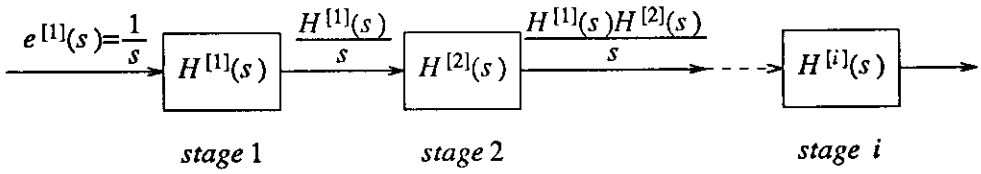

Fig. 1. Stages of *RC* Networks

It is this stage decomposition that enables us to write the excitation at the input of stage 2 as $\frac{H^{[1]}(s)}{s}$. Equation (10) suggests a very convenient way to handle the effect of non-unit-step input: simply analyze the network as if the input were a unit-step function, then evaluate the difference $\lim_{s \to 0}(\mathbf{u}(s) - \mathbf{1}e(s))$. The delay expression for stage one is given by:

$$\mathbf{T}_d^{[1]} = \mathbf{R}^{[1]}\mathbf{C}^{[1]}\,(\mathbf{1} - \mathbf{x}^{[1]}(0))\,,$$

and for stage 2,

$$\mathbf{T}_d^{[2]} = \mathbf{R}^{[2]}\mathbf{C}^{[2]}\,(\mathbf{1} - \mathbf{x}^{[2]}(0)) + \lim_{s\to 0}\,(\,\mathbf{u}(s) - \mathbf{1}\frac{H^{[1]}(s)}{s}\,)\,,$$

which is equal to,

$$\mathbf{T}_d^{[2]} = \mathbf{R}^{[2]}\mathbf{C}^{[2]}\,(\mathbf{1} - \mathbf{x}^{[2]}(0)) + \mathbf{1}T_c^{[1]}\,.$$

It is easy to see that in general for $i > 1$,

$$\mathbf{T}_d^{[i]} = \mathbf{R}^{[i]}\mathbf{C}^{[i]}\,(\mathbf{1} - \mathbf{x}^{[i]}(0)) + \mathbf{1}\sum_{k=1}^{i-1} T_c^{[k]}\,. \tag{11}$$

It follows that the delay calculation due to non-unit-step input is no harder than dealing with unit-step input.

V. Remarks and Conclusions

From a *model approximation* [11] point of view, defining delay as in (3) is equivalent to approximating the transfer function at each node by a first-order Padé approximation with the approximant $\hat{H}_i(s) = \dfrac{1}{s + \dfrac{1}{T_{ci}}}$. This approximant matches the first-order moment of the impulse response of $H_i(s)$. Since delays are *defined* in terms of the first-order moments of the impulse response, expression (8) follows naturally. As a matter of fact, the k^{th} moment of a system matrix **A** is given by $\mathbf{A}^{-(k+1)}\mathbf{b}$ [3].

To conclude, we have extended Elmore's delay to include a number of effects such as slow excitations which were not previously considered by others. This definition not only covers intrinsic and extrinsic delays, it also possesses a nice analytical property (11) simple enough for logic-level timing simulation.

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